

### 15.3 A 9.9G-10.8Gb/s Rate-Adaptive Clock and Data-Recovery with No External Reference Clock for WDM Optical Fiber Transmission.

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A clock and data recovery (CDR) circuit applicable for any bit-rate between 9.9G and 10.8Gb/s without external reference clock has been developed. A low phase noise dual-input voltage-controlled oscillator (VCO) which is insensitive to temperature, incorporates a fast tracking loop and a slow tracking loop combined with a DC gain enhancer (DCGE). This expands the capture range more than an order of magnitude, suppresses output jitter down to a quarter of conventional CDRs, and increases jitter tolerance. Consequently, 2mUIrms of jitter generation and 0.45UIpp of jitter tolerance have been achieved throughout 1GHz of capture range.

To comply with stringent SONET jitter specifications, a VCO in a CDR must be tuned to a frequency precisely identical to the received data rate. Thus, conventional CDRs operating at the 10Gb/s range [1][2] required external references such as a voltage-control crystal oscillator (VCXO), or their operation range were limited to a single rate. Although the data rate in a wavelength division multiplexing (WDM) optical fiber transmission which employs forward error correction (FEC) has been specified as 10.709Gb/s [3], existing data rates range from 9.95Gb/s without FEC to 10.8Gb/s depending on FEC algorithm. Therefore, CDR is required to support any rate between 9.9G and 10.8Gb/s. Moreover, to achieve a compact optical transceiver, it is desired to operate without external references.

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In order to meet the above requirements, a combined architecture of a fast and slow tracking loop, the DCGE, and the dual-input VCO is employed. The overall block diagram of the CDR with 1:16 demultiplexer (DMUX) is shown in Figure 15.3.1. The fast tracking loop consists of a phase detector (PD), an amplifier (AMP), a loop filter (FIL), and the VCO. The slow tracking loop consists of the PD, a frequency detector (FD), the DCGE, and the VCO. The circuit also contains 26dB limiting amplifier (LIM), 1:16 DMUX with LVDS interfaces, a loss-of-signal (LOS) indicator, and a loss-of-lock (LOL) indicator.

An analog type PD is used to obtain stable transfer characteristics. However, gain of the analog PD is generally low and cannot obtain enough open loop gain. To overcome this problem, the DCGE were adopted. The open and closed loop transfer characteristics are shown with a linear s-domain model in Figure 15.3.2. The DCGE increases open loop gain 32dB in low frequency range ( $f < 1\text{kHz}$ ), consequently suppressing the static phase error to be negligibly small. Therefore, the data can be sampled precisely at the center of the eye diagrams and the margin of jitter tolerance in high frequency range is maximized. The transfer characteristics depend on a cutoff frequency of the DCGE and a gain allocation to the AMP and the DCGE. These parameters were optimized so that the DCGE does not have any effect on the loop transfer response in the high frequency range ( $f > 10\text{kHz}$ ). Consequently, the peaking is kept 0.025dB at maximum in this design.

In the case of a CDR with low phase noise VCO, most (60-80%) of the jitter generations are caused by pattern dependent jitter. To reduce pattern dependent jitter, a center frequency of the VCO must be tuned precisely to the received data rate. The DCGE is capable of accumulating a long-term frequency deviation and retaining the control voltage for the VCO, and therefore preventing voltage fluctuation due to input data pattern. Thus, the DCGE suppresses pattern dependent jitter to become much less than conventional CDRs.

The FD detects beat frequency between the data rate and the frequency of the VCO and assists the loop in acquiring frequency lock and extending capture range. To obtain broad capture range, D-type flip-flops in the FD are designed to operate fast enough to sense high frequency components. In addition, the binary type FD is used so that the signal of FD does not fade away by the DCGE with a narrow bandwidth. A four-phase clock generator [4] is used as a delay circuit (DELY) to produce an exact 90deg. clock.

To obtain broad capture range, a VCO needs to cover wide frequency range. Thus, a high VCO gain is required. However, in a conventional CDR with a single-input VCO [5], wide loop bandwidth has been employed to satisfy SONET jitter tolerance spec. Therefore, noise generated in the PD and the FD was not eliminated by the loop and a higher VCO gain would lead to an increase of jitter. In the employed architecture with the dual-input VCO, loop bandwidth is determined by the fast tracking loop and the

bandwidth of the slow tracking loop can be set independently. Therefore, noise in high frequency range can be eliminated using the DCGE which has a narrow bandwidth, even when the VCO gain in slow tracking loop was set high. Consequently, the wide capture range is obtained without degrading jitter performance.

The circuit diagram of the dual-input VCO with a high-Q spiral inductor is shown in Figure 15.3.3. The oscillation frequency is determined by  $f_{vco} = 1/2\pi(L(Cc+Cf+Co+Cs))^{0.5}$ , where Cc is capacitance of varactor for coarse tuning, Cf is for fine tuning, Co is a fixed capacitance, and Cs is parasitic capacitance. Temperature dependence of oscillation frequency can be adjusted by a bias voltage Vbias. Due to the temperature compensation, less than 50MHz of frequency deviation has been achieved over 0-75deg range.

The CDR with 1:16 DMUX was fabricated in a 0.5 $\mu$ m SiGe BiCMOS process. Jitter performance was verified with the Anritsu MP1777A jitter analyzer. The output eye-diagram, jitter transfer and jitter tolerance characteristics are shown in Figure 15.3.4. More than 0.45UIpp of tolerance was achieved in 4-80MHz range. Figure 15.3.5 shows measured jitter generation vs. PRBS pattern length. The effect of the DCGE was confirmed by the comparison with the results without the DCGE. Figure 15.3.6 shows measured jitter generation vs. received data rate. A constant jitter generation was verified between 9.9G to 10.8Gb/s. A die micrograph is shown in Figure 15.3.7. The die size is 3.4x4.5mm<sup>2</sup>. Power consumption was 1.45W from 3.3V supply.

#### Acknowledgements:

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#### References:

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- [5] J. Savoj and B. Razavi, "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," ISSCC Digest of Technical Papers, pp.78-79, Feb. 2001

## Figure Caption List

Figure 15.3.1: Overall block diagram.

Figure 15.3.2: Open and closed loop transfer characteristics.

Figure 15.3.3: VCO circuit diagram.

Figure 15.3.4: Output eye-diagram, Jitter transfer and Jitter tolerance.

(Input: 10mVpp, 9.95328Gb/s, PRBS  $2^{31}-1$ )

Figure 15.3.5: Jitter generation vs. PRBS pattern length.

(Input: 10mVpp, 9.95328Gb/s, Jitter BW: 50k-80MHz)

Figure 15.3.6: Jitter generation vs. data rate.

(Input: 10mVpp, PRBS  $2^{31}-1$ )

Figure 15.3.7: Die micrograph.

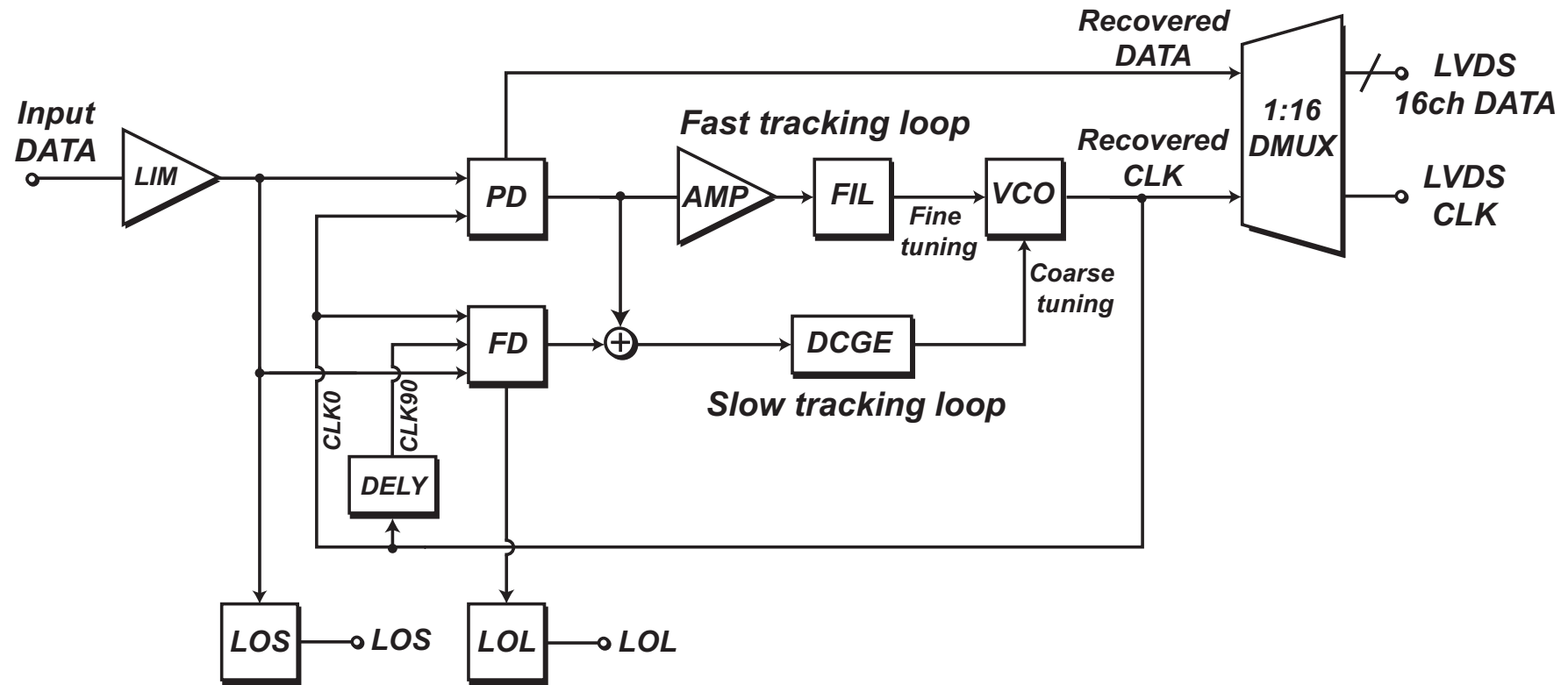
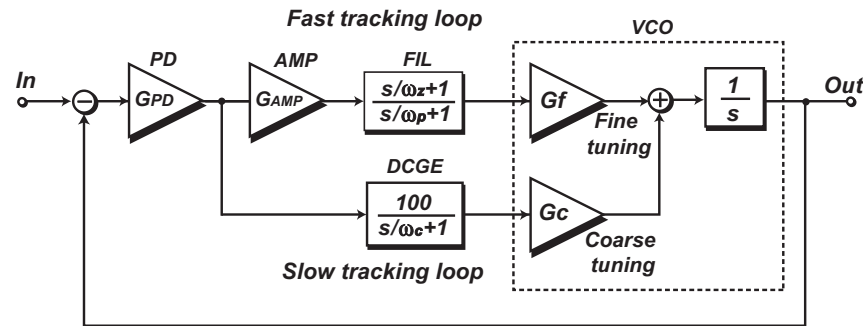


Figure 15.3.1: Overall block diagram.



PLL liner s-domain model

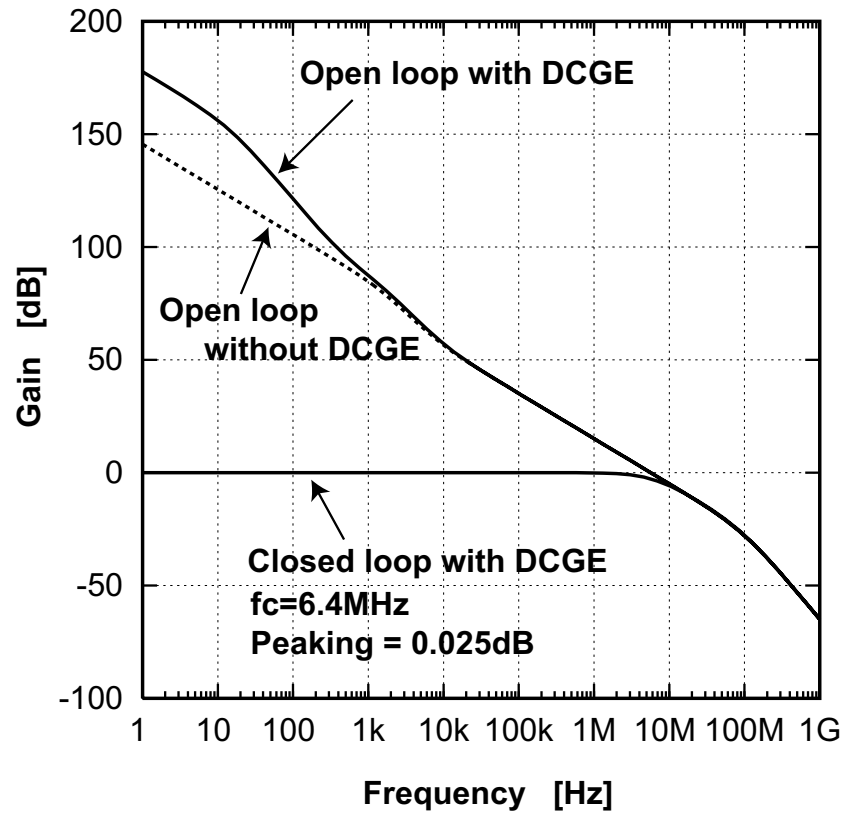
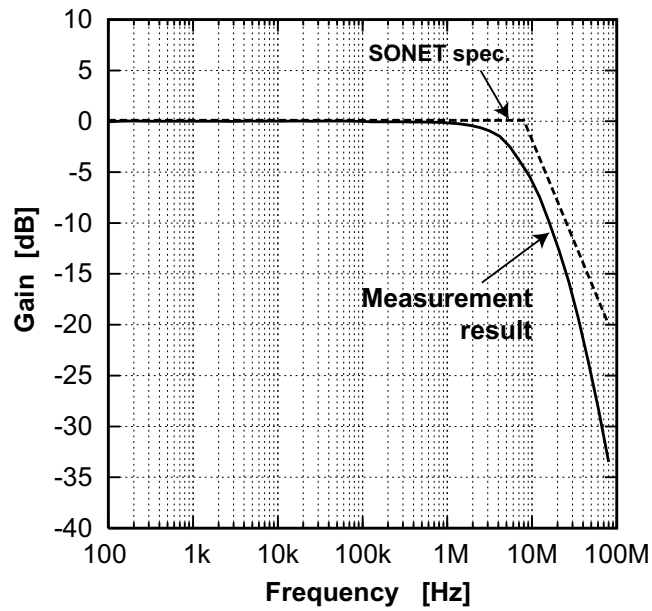
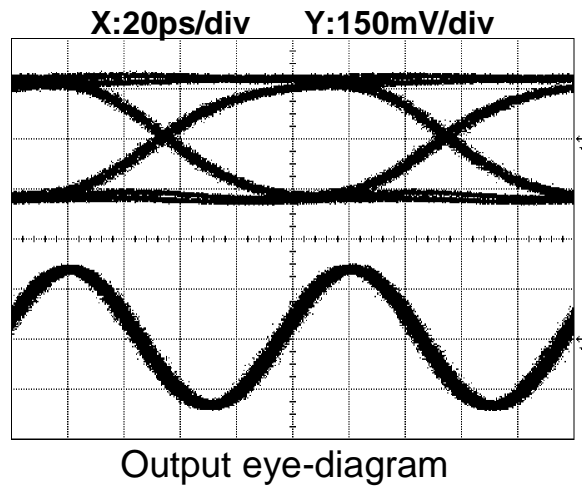
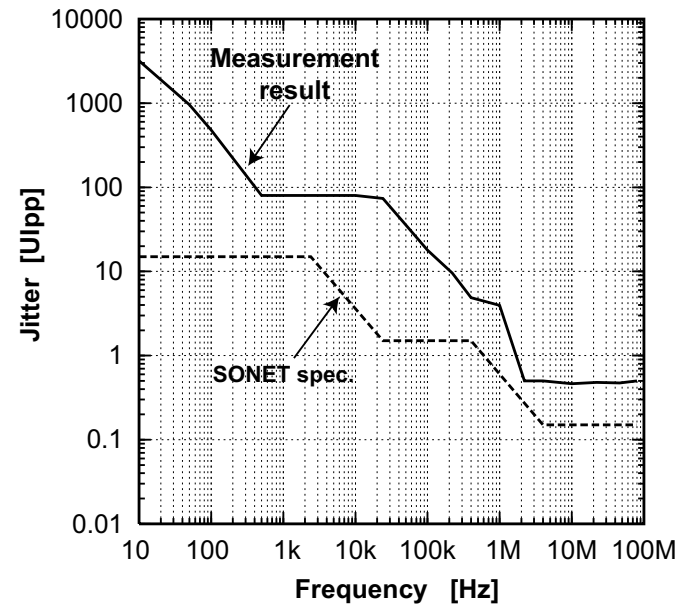


Figure 15.3.2: Open and closed loop transfer characteristics.



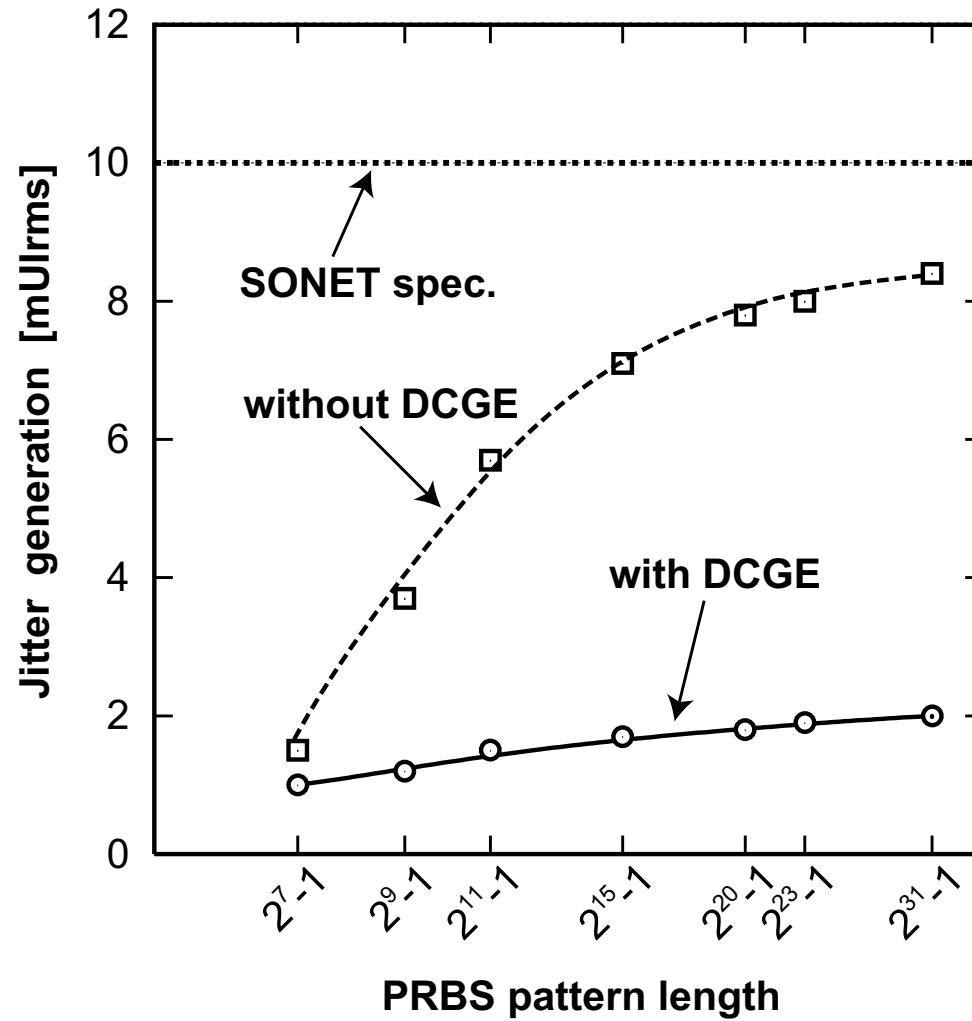


Jitter transfer

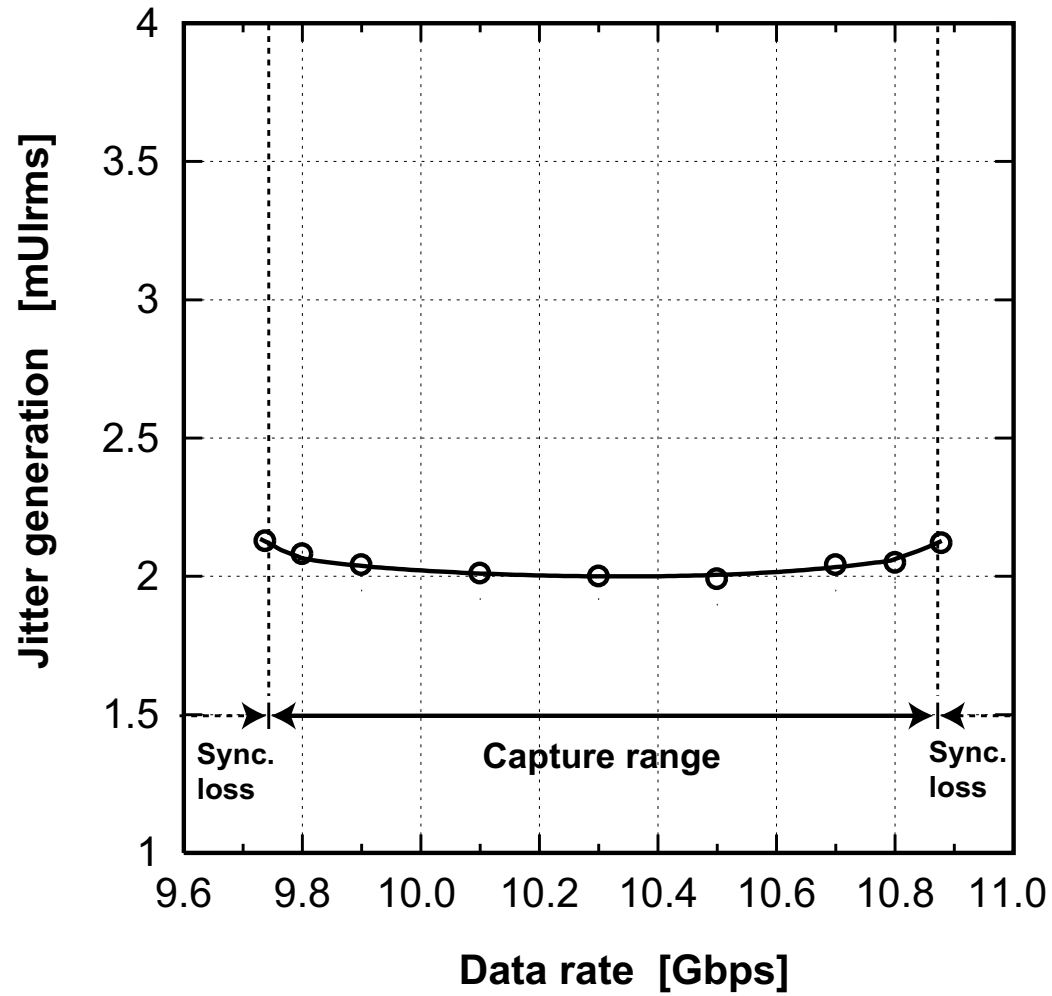


Jitter tolerance

**Figure 15.3.4: Output eye-diagram, Jitter transfer and Jitter tolerance.**  
 (Input: 10mVpp, 9.95328Gb/s, PRBS  $2^{31}-1$ )



**Figure 15.3.5: Jitter generation vs. PRBS pattern length.**  
 (Input : 10mVpp, 9.95328Gb/s, Jitter BW: 50k-80MHz)



**Figure 15.3.6: Jitter generation vs. data rate.**  
(Input : 10mVpp, PRBS 2<sup>31</sup>-1)

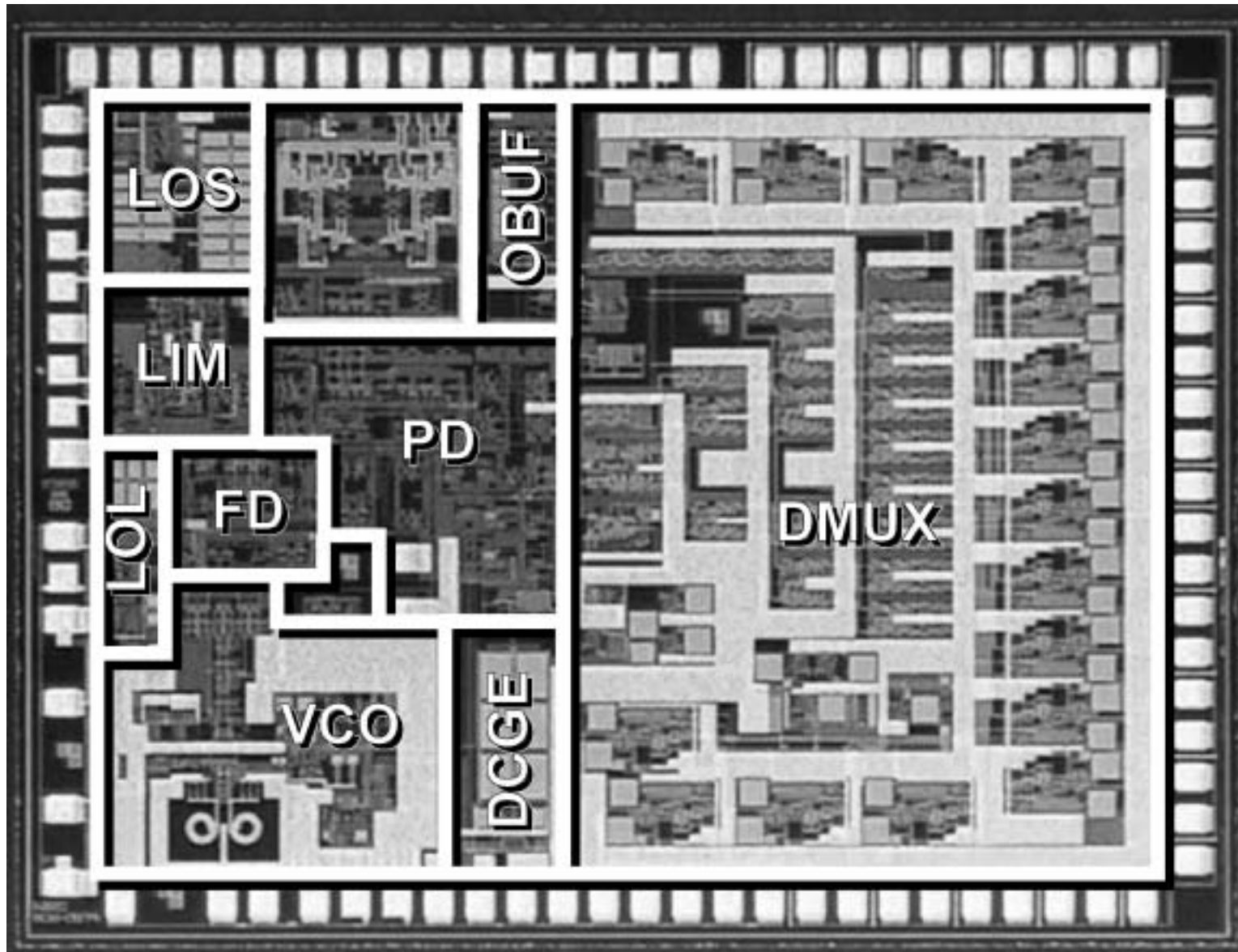


Figure 15.3.7: Die micrograph.