



## DS21354 & DS21Q354 E1 Transceivers

### REVISION A4 ERRATA

The errata listed below describe situations where DS21354 revision A4 and DS21Q354 revision A4 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor/Maxim intends to fix these errata in subsequent die revisions.

This errata sheet only applies to DS21354 revision A4 and DS21Q354 revision A4 components. Revision A4 components are branded on the topside of the package with a six-digit code of the form *yywwA4*, where *yy* and *ww* are two-digit numbers representing the year and work-week of manufacture, respectively. The die revision can also be determined through the lower four bits of the IDR register at location 0Fh. To obtain an errata sheet on another DS21354 or DS21Q354 die revision, see the Maxim website at [www.maxim-ic.com](http://www.maxim-ic.com), or contact technical support at [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

#### 1. TRANSMIT AND RECEIVE SIGNALING BUFFERS DO NOT OPERATE CORRECTLY IF INTERLEAVED BUS OPERATION (IBO) IS ENABLED

##### Description

If interleaved bus operation is enabled, hardware signaling using the TSIG and RSIG pins is not available, the Receive Signaling Change (RSC) interrupt does not operate and signaling reinsertion in the receive path is non-functional.

##### Work-around

Do not use hardware signaling in interleaved bus operating mode. Other functionality associated with interleaved bus operation is still available. The device will correctly interleave the serial data streams at RSER and signaling is available in the Receive Signaling Registers. Changes in signaling states can still be identified in software by reading the Receive Signaling Registers each multiframe and comparing the contents with the previous multiframe of signaling.

#### 2. PROPAGATION DELAYS EXCEED DATA SHEET LIMITS

##### Description

The propagation delays,  $T_{D1}$ ,  $T_{D2}$ ,  $T_{D3}$  and  $T_{D4}$ , exceed the limits set forth in the data sheet for the 3.3 volt operation. The data sheet specifies 50ns max.  $T_{D1}$  and  $T_{D2}$  can be as long as 65ns.  $T_{D3}$  and  $T_{D4}$  are typically 60ns to 90ns.

##### Work-around

In applications using the elastic store buffers and an 8.192 MHz back plane clock, the RSER output is delayed such that the output could transition during the falling edge of the clock. This could result in other devices on the back plane latching the bit during the transition of the output driver. It is recommended that the 8.192 MHz clock applied to the RSYCLK input pin be inverted. This will move the data one half-clock cycle so that the data bits can be latched by other devices on the falling edge of the uninverted clock. Operation at slower back plane clock speeds are unaffected.

### 3. IT IS POSSIBLE FOR THE 8MCLK PIN TO OUTPUT 24.576 MHz ON POWER-UP

#### Description

It is possible for the 8MCLK pin to output 24.576 MHz on Power-up.

#### Work-around

To avoid this situation, reset the PLL by writing a 01h into location ACh. After 1ms, clear the reset bit by writing a 00h into location Ach.

### 4. DURING JTAG OPERATION, THE JTDO PIN WILL TRANSITION ON THE FALLING EDGE OF JTCLK

#### Description

The JTDO pin transitions with the falling edge of JTCLK, rather than the next rising edge.

#### Work-around

To remove the possibility of misinterpretation of the data output, it is recommended that a .001 uF capacitor be placed from JTDO to ground.

### 5. EQUALIZER GAIN LIMIT

#### Description

When using the Equalizer Gain Limit (EGL) function (bit LICR.4 = 0), the receiver may squelch an input signal with more than -7.5dB of attenuation.

#### Work-around

For signals in the -7.5dB to -12dB range, set the EGL bit to 1. No other known work around exists for this errata.

### 6. NEW FEATURE ADDED IN REVISION B1

#### Description

The "Receive Monitor Mode" included in the released data sheet became an official feature with the B1 die revision. This feature was purposefully omitted from prior versions of the data sheet because the mode was experimental and early revisions of the device did not meet the intended objectives. Once the B1 revision had been evaluated and found to function properly, the feature was added to the data sheet.

### 7. INCORRECT ERROR COUNT REPORTED IN ERROR COUNT REGISTERS

#### Description

The error count registers may report an error count that is one error higher than the actual error count due to a potential internal collision at the one-second timer boundary during data transfer from the error counter to the error count register. The actual error count internal to the part will be accurate in this situation and all re-sync criteria will be followed correctly, but the error count registers may report an error count that is one error higher than the actual error count.

#### Work-around

None.