



Low RON, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

General Description

The MAX4991–MAX4994 low on-resistance analog switches operate from a single +1.8V to +5.5V supply. The MAX4991/MAX4993 feature a slow turn-on time to reduce clicks and pops due to coupling capacitors and audio amplifiers with a DC output bias. This feature provides click-and-pop reduction without adding additional parts for existing architectures.

The MAX4991/MAX4992 are dual single-pole/double-throw (SPDT) switches, while the MAX4993/MAX4994 are double-pole/double-throw (DPDT) switches. The MAX4993/MAX4994 feature an active-low enable input (EN) that sets all the channels to high impedance and reduces supply current when driven high. These devices have 0.3Ω on-resistance and 0.004% THD+N to route high fidelity audio signals.

The MAX4991–MAX4994 are available in space-saving 10-pin UTQFN (1.4mm x 1.8mm) package, and are specified for operation over the -40°C to +85°C extended temperature range.

Applications

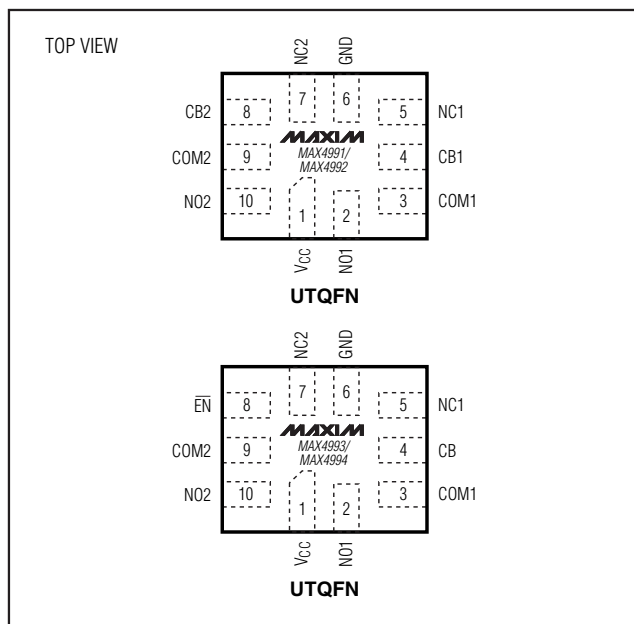
Speaker Headset Source Switching
Cellular Phones
Portable MP3 Players
Audio Signal Routing

Typical Application Circuit appears at end of data sheet.

Features

- ◆ Slow Turn-On for Click-and-Pop Reduction Without Additional Parts
- ◆ Low 0.3Ω On-Resistance
- ◆ Low RON Flatness (1mΩ)
- ◆ Low THD+N: 0.004%
- ◆ +1.8V to +5.5V Single-Supply Operation
- ◆ 1.2μA (typ) Supply Current
- ◆ Space-Saving Packages
10-Pin UTQFN (1.4mm x 1.8mm x 0.55mm)

Pin Configurations



MAX4991–MAX4994

Ordering Information/Selector Guide

| PART | PIN-PACKAGE | CONFIGURATION | SLOW-SWITCHING TIME | ENABLE LINE | TOP MARK |
|--------------|-------------------|---------------|---------------------|-------------|----------|
| MAX4991EVB+* | 10 Ultra-Thin QFN | Dual SPDT | Yes | No | AAD |
| MAX4992EVB+ | 10 Ultra-Thin QFN | Dual SPDT | No | No | AAE |
| MAX4993EVB+ | 10 Ultra-Thin QFN | DPDT | Yes | Yes | AAF |
| MAX4994EVB+* | 10 Ultra-Thin QFN | DPDT | No | Yes | AAG |

Note: All devices operate over -40°C to +85°C extended temperature range.

+Denotes a lead-free package.

*Future product—contact factory for availability.



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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

| | |
|---|---|
| V _{CC} , CB ₋ , EN |-0.3V to +6.0V |
| COM ₋ , NC ₋ , NO ₋ | -0.3V to (V _{CC} + 0.3V) |
| Continuous Current COM ₋ , NC ₋ , NO ₋ |±350mA |
| Peak Current COM ₋ , NC ₋ , NO ₋ (pulsed at 1ms, 50% duty cycle) |±700mA |
| Peak Current COM ₋ , NC ₋ , NO ₋ (pulsed at 1ms, 10% duty cycle) |±1.5A |
| Continuous Power Dissipation (T _A = +70°C) | |
| 10-Pin UTQFN (derate 6.9mW/°C above +70°C) |559mW |

Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)

10-Pin UTQFN20.1°C/W

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)

10-Pin UTQFN143.1°C/W

Operating Temperature Range-40°C to +85°C

Junction Temperature Range+150°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10s)+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|---|--|---|-----|-----------------|-------------------|
| Power-Supply Range | V _{CC} | | 1.8 | | 5.5 | V |
| Undervoltage Lockout | V _{UVLO} | | | 1.4 | | V |
| Supply Current (MAX4991/MAX4992) | I _{CC} | VCB1 = VCB2 = 0V or V _{CC} | V _{CC} = 3V | 1.2 | 2.5 | μA |
| | | | V _{CC} = 5.5V | 3.1 | 6 | |
| | | VCB1 = VCB2 = 0.5V or 1.4V | V _{CC} = 2.7V | | 3 | |
| | | | V _{CC} = 5.5V | | 14 | |
| Supply Current (MAX4993/MAX4994) | I _{CC} | VEN = V _{CC} , VCB = 0V or V _{CC} | V _{CC} = 5.5V | 0.1 | 1 | μA |
| | | | V _{CC} = 3V | 1.2 | 2.5 | |
| | | VEN = 0V, VCB = 0V or V _{CC} | V _{CC} = 5.5V | 3.1 | 6 | |
| | | | V _{CC} = 2.7V | | 3 | |
| | | VEN = VCB = 0.5V or 1.4V | | 8.5 | | |
| Power-Supply Rejection Ratio | PSRR | R _L = R _S = 50Ω, f = 20kHz | | 80 | | dB |
| Analog Signal Range | V _{NC-} , V _{NO-} , V _{COM-} | | 0 | | V _{CC} | V |
| On-Resistance | R _{ON} | V _{CC} = 2.7V, V _{NC-} or V _{NO-} = 0 to V _{CC} , I _{COM-} = 100mA | T _A = +25°C | 0.3 | 0.5 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 0.6 | |
| On-Resistance Match Between Channels | ΔR _{ON} | V _{CC} = 2.7V, between NC ₋ , NO ₋ only, I _{COM-} = 100mA, V _{NC-} or V _{NO-} = V _{CC} /2 | | 3 | | mΩ |
| On-Resistance Flatness | R _{FLAT} | V _{CC} = 2.7V, V _{NC-} or V _{NO-} = 0 to V _{CC} , I _{COM-} = 100mA (Note 3) | | 1 | | mΩ |
| COM ₋ Output Noise | N _{COM-} | V _{NC-} = V _{NO-} = 0, R _L = 50Ω | f = 20Hz–20kHz | 1 | | μV _{RMS} |
| | | | f = 0Hz–1MHz | 50 | | |

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MAX4991-MAX4994

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|------|-------|------|---------|
| NC_, NO_ Off-Leakage Current | $I_{L(OFF)}$ | $V_{CC} = 2.7V$, switch open, $V_{NC_}$ or $V_{NO_} = 0$ or V_{CC} , $V_{COM_} = V_{CC}$ or 0 | -100 | | +100 | nA |
| COM_ Off-Leakage Current (MAX4993/MAX4994) | $I_{COM_L(OFF)}$ | $V_{CC} = 2.7V$, $V_{EN} = V_{CC}$, $V_{NC_}$ or $V_{NO_} = 0$ or V_{CC} , $V_{COM_} = V_{CC}$ or 0 | -100 | | +100 | nA |
| COM_ On-Leakage Current | $I_{COM_L(ON)}$ | $V_{CC} = 2.7V$, switch closed, $V_{NC_}$ or $V_{NO_} = 0$, V_{CC} or unconnected, $V_{COM_} = 0$, V_{CC} , or unconnected | | 60 | 140 | nA |
| DYNAMIC | | | | | | |
| Turn-On Time (Note 4) (Figure 1) | t_{ON} | $V_{CC} = 2.7V$, $V_{NC_}$ or $V_{NO_} = 1.5V$, $R_L = 50\Omega$, $C_L = 35pF$ (MAX4991/MAX4993) | 120 | 360 | 630 | ms |
| | | $V_{CC} = 2.7V$, $V_{NC_}$ or $V_{NO_} = 1.5V$, $R_L = 50\Omega$, $C_L = 35pF$ (MAX4992/MAX4994) | | 20 | 150 | μs |
| Turn-Off Time | t_{OFF} | $V_{CC} = 2.7V$, $V_{NC_}$ or $V_{NO_} = 1.5V$, $R_L = 50\Omega$, $C_L = 35pF$ Figure 1 (Note 4) | | 0.5 | 2 | μs |
| Off-Isolation | V_{ISO} | $R_S = R_L = 50\Omega$, $f = 20kHz$, $V_{COM_} = 1VP-P$, Figure 2 (Note 5) | | -90 | | dB |
| Crosstalk | V_{CT} | $R_S = R_L = 50\Omega$, $f = 20kHz$, $V_{COM_} = 1VP-P$, Figure 2 (Note 6) | | -110 | | dB |
| Total Harmonic Distortion | THD+N | $f = 20Hz$ to $20kHz$, $V_{COM_} = 0.5VP-P$, $R_S = R_L = 50\Omega$, DC bias = 0 | | 0.004 | | % |
| NC_, NO_ Off-Capacitance | C_{OFF} | $COM_ = GND$ (DC bias), $f = 1MHz$, $V_{NO(NC)} = 100mVP-P$, (Figure 3) | | 45 | | pF |
| COM_ On-Capacitance | C_{ON} | $COM_ = GND$ (DC bias), $f = 1MHz$, $V_{COM} = 100mVP-P$ (Figure 3) | | 65 | | pF |
| DIGITAL I/O (CB, CB1, CB2, EN) | | | | | | |
| Input Logic-High | V_{IH} | | 1.4 | | | V |
| Input Logic-Low | V_{IL} | | | | 0.5 | V |
| Input Leakage Current | I_{CB} | $V_{CB_} = V_{EN} = 0V$ or V_{CC} | -1 | | +1 | μA |

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

Note 3: Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog ranges.

Note 4: All timing is measured using 10% and 90% levels.

Note 5: Off-isolation = $20\log [V_{COM_}/(V_{NO_}$ or $V_{NC_})]$, $V_{COM_}$ = output, $V_{NO_}$ or $V_{NC_}$ = input to off switch.

Note 6: Between any two switches.

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Test Circuits/Timing Diagrams

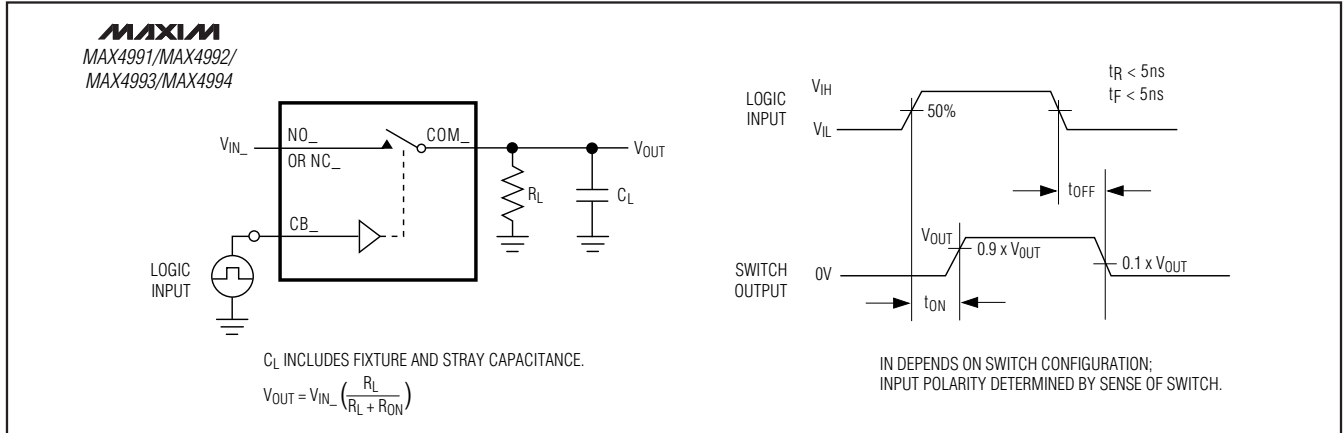


Figure 1. Switching Time

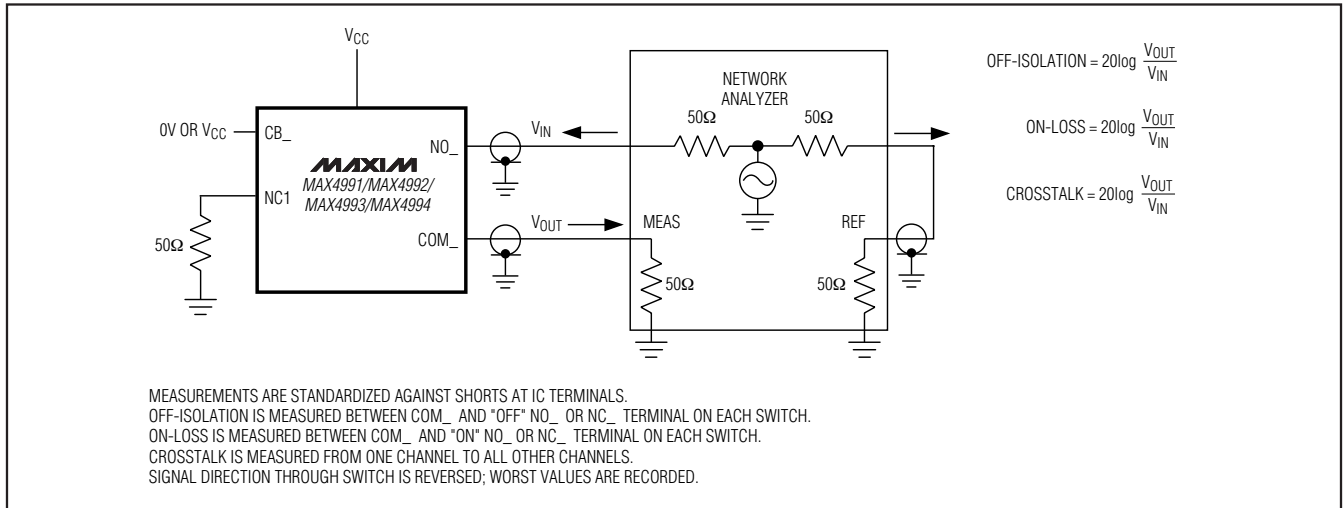


Figure 2. On-Loss, Off-Isolation, and Crosstalk

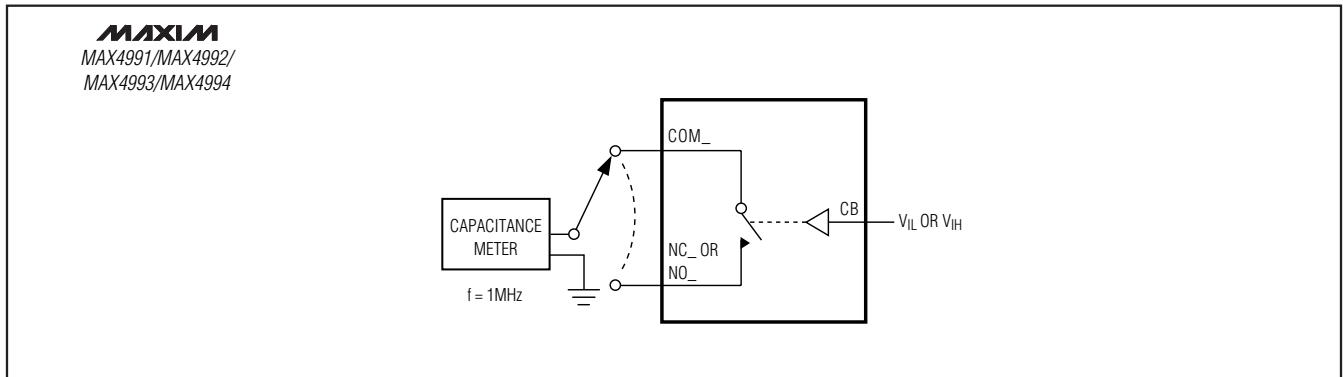


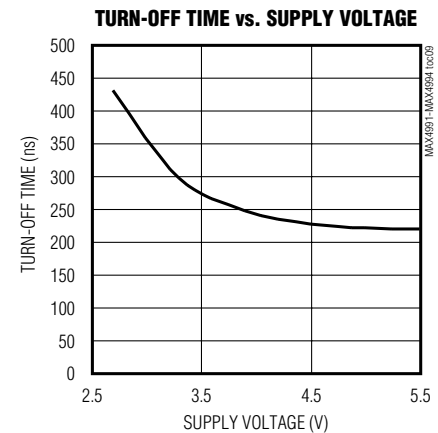
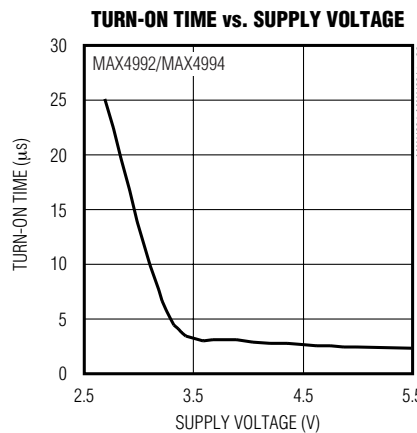
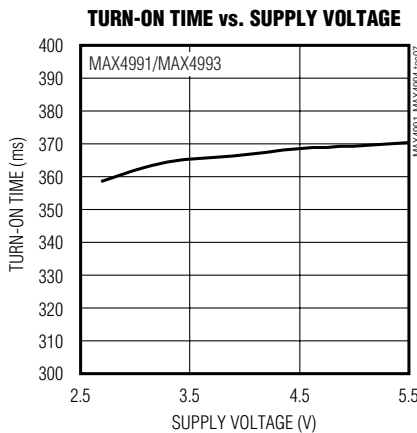
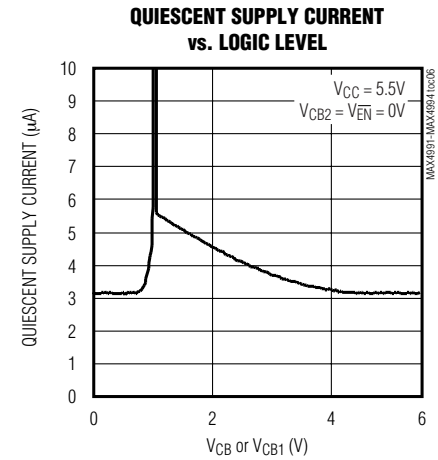
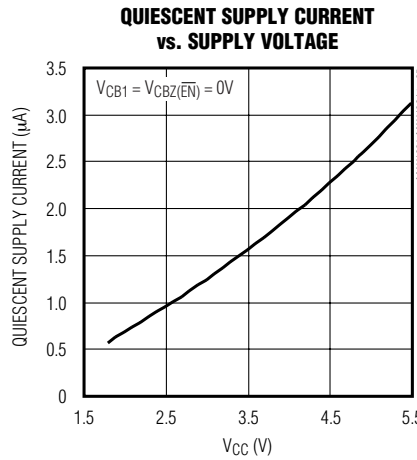
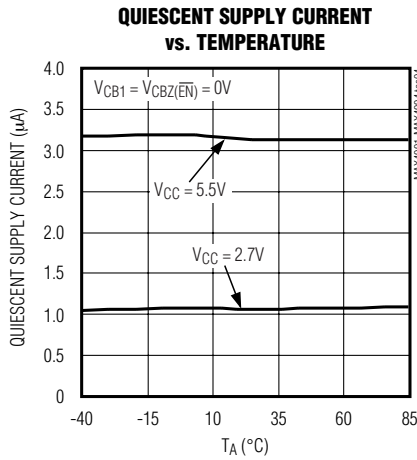
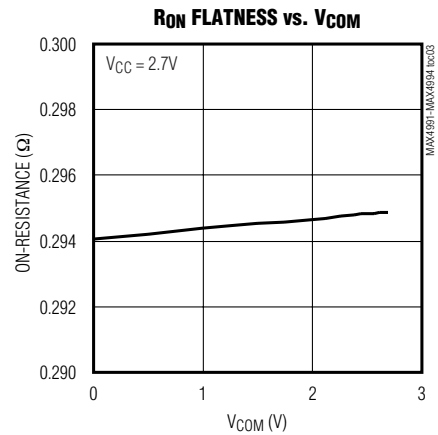
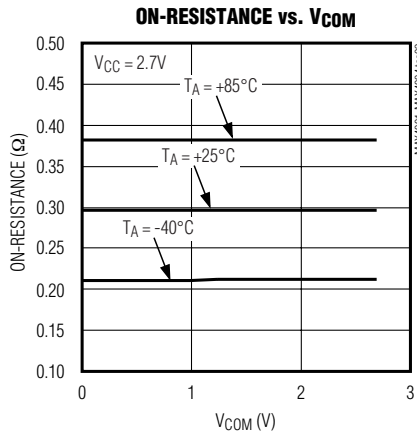
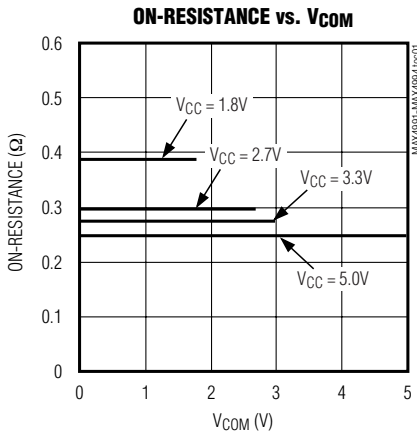
Figure 3. Channel Off-/On-Capacitance

Low Ron, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Typical Operating Characteristics

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

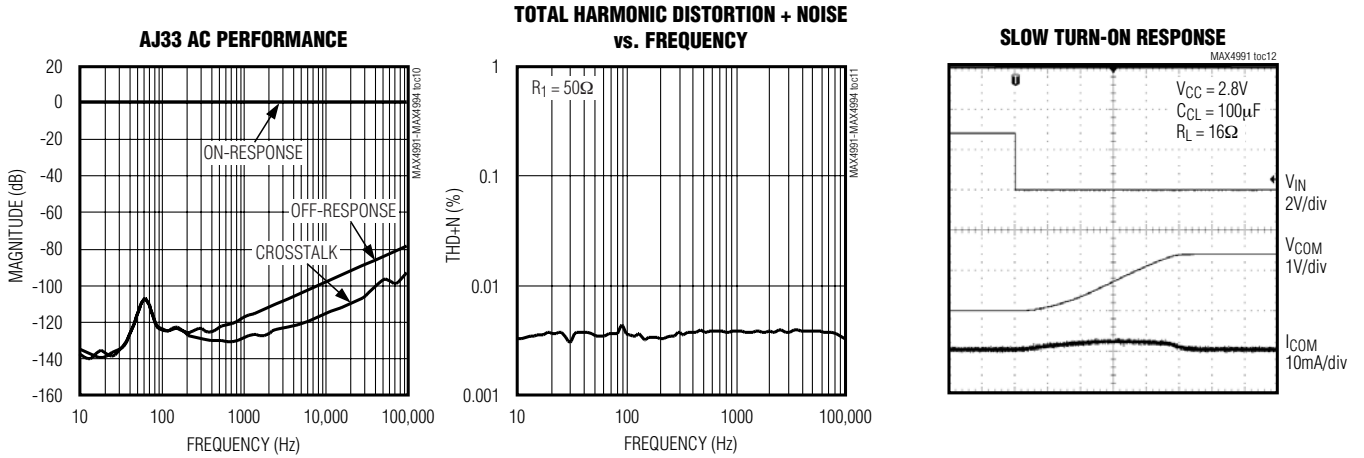
MAX4991-MAX4994



Low RON, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Typical Operating Characteristics (continued)

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



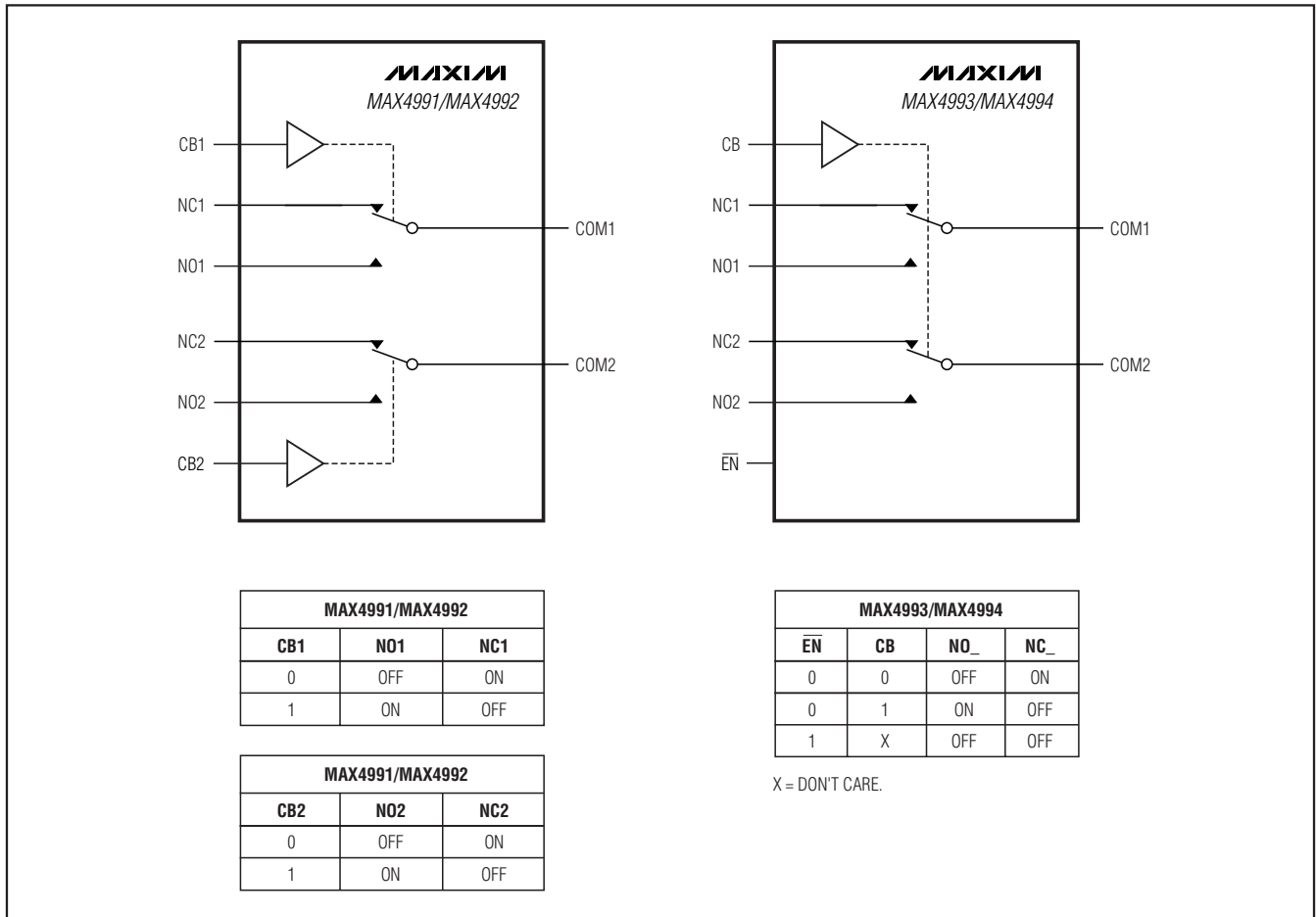
Pin Description

| PIN | | NAME | FUNCTION |
|-----------------|-----------------|-----------------|---|
| MAX4991/MAX4992 | MAX4993/MAX4994 | | |
| 1 | 1 | V_{CC} | Positive-Supply Voltage Input. Bypass V_{CC} to GND with a $0.1\mu F$ capacitor as close as possible to the device. |
| 2 | 2 | NO1 | Analog Switch 1—Normally Open Terminal |
| 3 | 3 | COM1 | Analog Switch 1—Common Terminal. COM1 must be connected to the speaker load for click-and-pop reduction. |
| 4 | — | CB1 | Digital Control Input for Switch 1 |
| — | 4 | CB | Digital Control Input for Switch 1 and Switch 2 |
| 5 | 5 | NC1 | Analog Switch 1—Normally Closed Terminal |
| 6 | 6 | GND | Ground |
| 7 | 7 | NC2 | Analog Switch 2—Normally Closed Terminal |
| 8 | — | CB2 | Digital Control Input for Switch 2 |
| — | 8 | \overline{EN} | Active-Low Enable Input—Drive \overline{EN} high to put switches in high impedance. Drive \overline{EN} low for normal operation. |
| 9 | 9 | COM2 | Analog Switch 2—Common Terminal. COM2 must be connected to the speaker load for click-and-pop reduction. |
| 10 | 10 | NO2 | Analog Switch 2—Normally Open Terminal |

Low Ron, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Functional Diagram

MAX4991-MAX4994



Detailed Description

The MAX4991-MAX4994 low 0.3Ω (typ) on-resistance analog switches have break-before-make switching and operate from a single +1.8V to +5.5V supply. The MAX4991/MAX4993 provide a slow turn-on time, and with COM_ used as the output, reduce clicks and pops due to coupling capacitors and audio amplifiers with a DC output bias. This feature is important for existing architectures with coupling capacitors at the output that need click-and-pop reduction.

The MAX4993/MAX4994 DPDT switches with an active-low enable input (\overline{EN}) set all channels to high impedance and reduce supply current when driven high. The MAX4991-MAX4994 have a low 0.004% THD+N to route high-fidelity audio signals.

Digital Control Input

The MAX4991/MAX4992 have two digital control logic inputs, CB1 and CB2. The MAX4993/MAX4994 have a single digital-control logic input, CB. The digital control logic inputs control the position of the corresponding switch as shown in the *Functional Diagram*. Driving logic inputs rail-to-rail minimizes power consumption.

Enable Input (MAX4993/MAX4994)

The MAX4993/MAX4994 feature an active-low enable input (\overline{EN}). When \overline{EN} is driven high, the switches are high impedance and reduce supply current. When \overline{EN} is driven low, the MAX4993/MAX4994 operate in normal mode. Driving \overline{EN} rail-to-rail minimizes power consumption.

Low RON, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Analog Signal Levels

The MAX4991–MAX4994 have a very low and stable R_{ON} , 0.3Ω (typ), as the analog input signals are swept from ground to V_{CC} (see *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_+ , NC_+ , and COM_+ to be configured as either inputs or outputs; however, click-and-pop reduction is only operational when COM_+ is used as the output.

Power-Supply Rejection Ratio

PSRR is the measurement of AC power-supply ripple or noise that couples to the output. Variations in supply voltage corrupt the audio signal due to changes in the R_{ON} value by supply modulation. The MAX4991–MAX4994 maintain a 80dB (typ) PSRR across the supply-voltage range, eliminating any corruption of the audio signal from supply variations. Therefore, with no audio signal, the R_{ON} variation due to supply-voltage ripple does not contribute to any output signal modulation.

Applications Information

Click-Pop Reduction

The MAX4991/MAX4993 feature a slow switch turn-on that can reduce click-and-pop noise caused by abrupt changes in voltage across a speaker. These voltage

changes usually occur when a single-supply audio amplifier with a DC bias is turned on, causing a spike of current in the speaker while the coupling capacitor charges (see the *Typical Operating Circuit*). If the audio amplifier connected to the unused input is powered up before the switch position changes, the MAX4991/MAX4993 reduce the current spike to COM_+ . The speaker load must be present so that the current charging the coupling capacitor has a path to ground.

Layout

Good layout improves performance by decreasing the amount of stray capacitance and noise. Minimize PCB trace lengths and resistor leads and place external components as close as possible to the device.

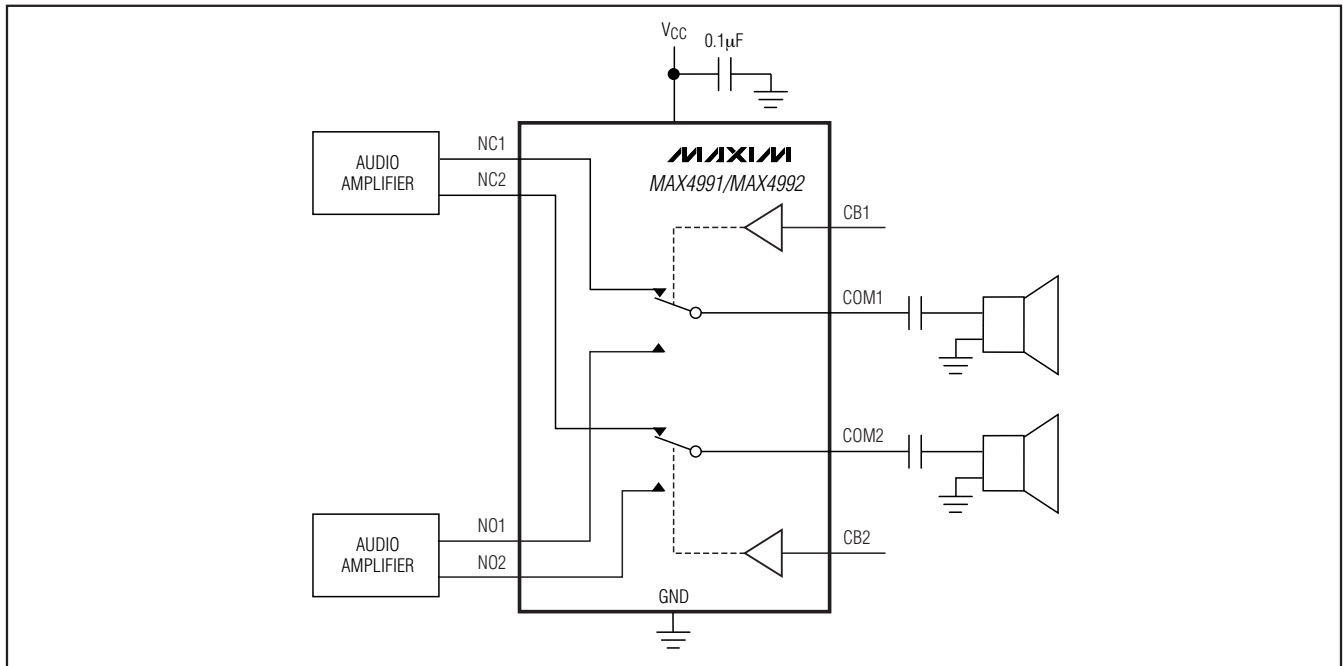
Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying analog signals especially if the analog signal is not current limited.

Low Ron, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Typical Operating Circuit



MAX4991-MAX4994

Chip Information

PROCESS: BiCMOS

Low RON, Dual-SPDT/Single-DPDT Analog Switches with Slow Turn-On Time

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---------------------|---------------------|-------------------------|
| 10 Ultra-Thin QFN | V101AICN-1 | 21-0028 |

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