



## APPLICATION NOTE 986

# Input and Output Noise in Buck Converters Explained

*Abstract: Input and output noise in buck (step-down) converters can be a cause of concern to the system designer. This application note attempts to provide a theoretical explanation of the individual contributions of conducted noise on the input and output sides of buck converters. These equations will hopefully allow the power supply design optimize components for noise immunity.*

## Introduction

The goal of this application note is to give a brief explanation of the individual contributions of conducted noise on the input and output sides of buck (step-down) converters. Equations are listed to help calculate the peak-to-peak noise contributions of each noise source. These equations will hopefully allow the designer of buck converters to pick components that will help them meet their design objectives.

## Assumptions

The equations listed in this application note are appropriate for any buck converter, independent of the control scheme, as long as they meet the following limitations:

### 1) The equations assume continuous conduction above 0A.

This assumption describes the current flow in the inductor. Depending on the components used, the load and the topology of the buck converter, the current flow through the inductor can look like that shown in **Figure 1**. The middle graph of Figure 1 shows discontinuous current flow. Discontinuous current flow occurs when the current through the inductor tries to go negative (current flows out of the output capacitor and into ground), but gets clamped at zero. Discontinuous conduction typically, but not always, occurs under light load conditions.

The bottom graph of Figure 1 shows an example of continuous conduction where the current through the inductor drops below 0A. In order for the current to drop below 0A, the converter needs to have synchronous rectification and be designed to allow for such operation. With such a converter the current will typically, but not always, go below 0A under light load conditions.

Independent of whether the converter is synchronously rectified or not, continuous conduction above 0A will tend to happen at higher loads as shown in the top graph in Figure 1. Thus, the equations listed in this application note should be appropriate when the converter is operating close to maximum loading.

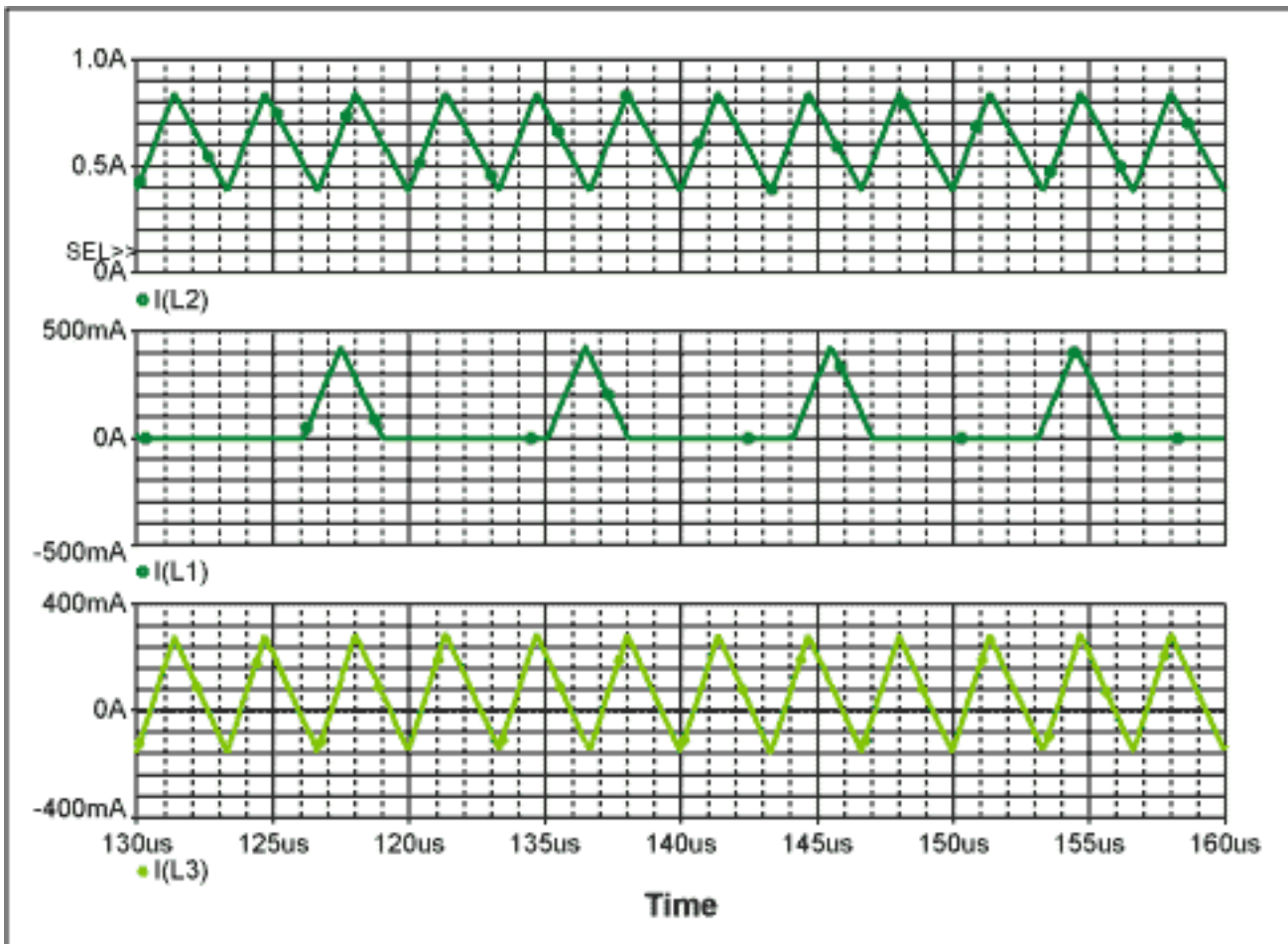


Figure 1. Shows three possible waveforms for the current flowing through the inductor in a buck converter. The top graph shows continuous conduction operation where the current never drops below 0A. The middle graph shows discontinuous conduction. The bottom graph shows continuous conduction where the current drops below 0A.

Use the equation listed below to test a particular design. If this inequality is met, the converter is operating in continuous conduction above 0A, and this first assumption will be satisfied.

$$\left( i_{\text{out}} - \frac{1}{2 \cdot f \cdot L} \cdot \frac{V_{\text{out}}}{V_{\text{in}}} \cdot (V_{\text{in}} - V_{\text{out}}) \right) > 0$$

$V_{\text{in}}$  = the input voltage

$V_{\text{out}}$  = the output voltage

$f$  = the frequency at which the buck regulator is switching

$L$  = the value of the inductor

$i_{\text{out}}$  = the output current

Equation 1. When this equation is met, an ideal buck converter will be operating in continuous conduction with the current through the inductor never going below ground.

## 2) The load is a constant DC load

This assumption needs to be made for practical reasons. While assumption #1 is a reasonable assumption for most applications, this assumption is most likely not true. In a typical buck converter application the current draw of the load will fluctuate. This fluctuation will cause noise, due to the finite response time of the converter,

and the equivalent series resistance (ESR) of the output capacitor (explained later), among other things. In order to calculate the output noise due to this fluctuation, the characteristics of the load need to be known. For the purposes of this application note, this is, of course, impossible.

### 3) The converter is 100% efficient

This again is a practical consideration. The equations would be unwieldy if this assumption was not made. Most modern buck converters have excellent efficiency and the amount of error this assumption introduces is minimal.

## Background

Some of the noise sources in buck converters come from the non-ideal properties of the components used. To better understand these noise sources, a brief discussion of the non-ideal aspects of components are discussed below. To keep this discussion simple, only the non-idea properties relative to buck converters are discussed.

### Model for MOSFETs

For the purposes of a buck converter, a first-order model for a MOSFET is a switch in series with a resistance, as shown in **Figure 2**. In this model, the MOSFET has a finite resistance between its drain and its source when the MOSFET is turned on. Typical on resistances can vary widely depending on the MOSFET and the application. As a point of reference, the IRF7303 used on the MAX1653EVM has a typical on-resistance of  $.08 \Omega$  ( $V_{gs} = 4.5V$ ).

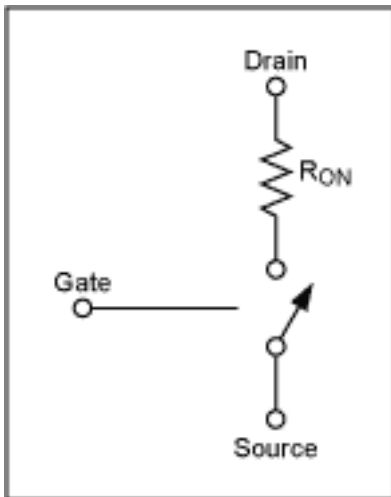


Figure 2. A first-order model of a MOSFET used in a buck converter.

A more complete model for a MOSFET is shown in **Figure 3**.

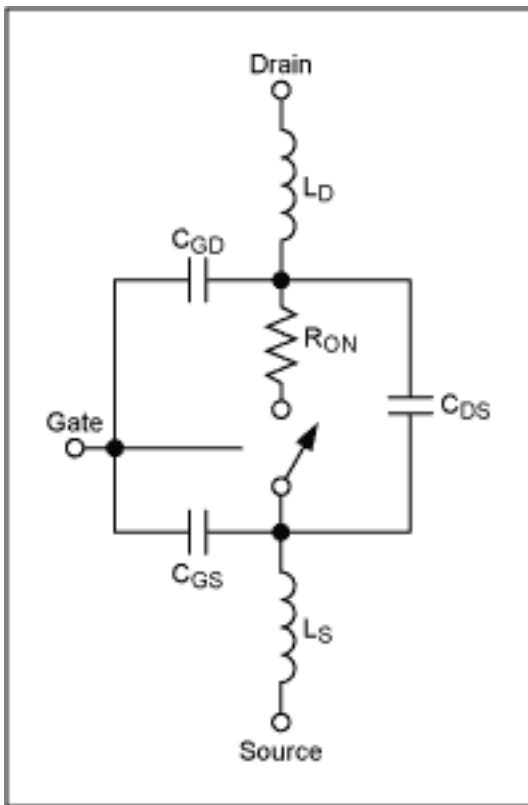


Figure 3. A more detailed model of a MOSFET used in a buck converter.

This model adds inductances and capacitances to the first-order model in Figure 2. The three capacitors shown are:

- $C_{gd}$  = Capacitance from the gate to the drain
- $C_{gs}$  = Capacitance from the gate to the source
- $C_{ds}$  = Capacitance from the drain to the source

Again, using the IRF7303 as an example, typical values for these capacitances are listed below ( $V_{ds} = 8V$ ).

- $C_{gd} = 120pF$
- $C_{gs} = 470pF$
- $C_{ds} = 180pF$

In addition to these capacitances, both the drain and the source of the MOSFET have equivalent inductances in series with them. In the case of the IRF7303, these are both listed in the data sheet of the IRF7303 as 4nH and 6nH for the drain and source respectively.

## Model for Capacitors

The model for a capacitor is shown in **Figure 4**.

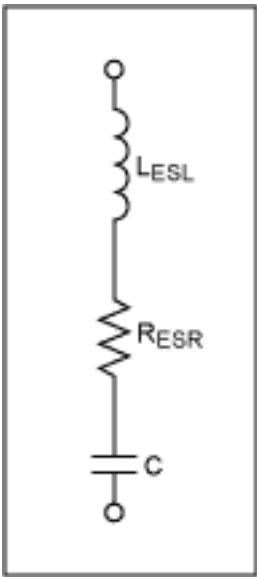


Figure 4. A model for capacitors used in buck converters.

All capacitors have what looks like a resistor in series with its capacitance. This resistor is referred to as the equivalent series resistance (ESR) of the capacitor. This ESR varies significantly with the type of capacitor used. Ceramic capacitors typically have very low ESR, the average Aluminum Electrolytic capacitor can have high values of ESR, with Tantalums somewhere in between. In recent years, there have been a number of specially made capacitors designed to minimize ESR. Below is a small listing of some examples:

- AVX TPS series. Example: 10V, 100uF capacitor with an ESR as low as .065  $\Omega$  at 100kHz
- Kemet A700 series. Example: 6.3V, 100uF capacitor with an ESR as low as .03  $\Omega$  max at 100kHz
- Panasonic ECJ series. Example: 16V, 4.7uF capacitor with an ESR as low as .017  $\Omega$  max at 100kHz

Note that the ESR of a capacitor varies with frequency.

Also in this model is the equivalent series inductance (ESL) of the capacitor. Some typical inductances for ceramic chip capacitors are listed below:

.1uF at 1.7nH  
 .01uF at .84nH  
 1000pF at 1.7nH

Values for Tantalum and Aluminum capacitors are more difficult to come by, but are probably on the order of 5nH to 10nH for a good high value, surface mount capacitor.

## Model for a Reversed Bias Diode

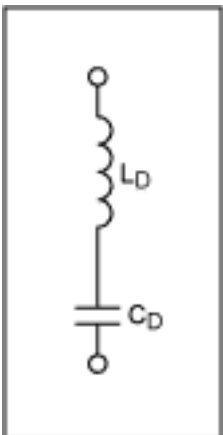


Figure 5. A model for reversed biased diode used in a buck converter.

The catch diode used on some buck converters can be modeled as an inductance in series with a capacitor when

reversed biased. The MBR030 used on the MAX1653EVMKit has a capacitance of approximately 55pF when reversed biased with 8V. This capacitance varies significantly with bias voltage. The inductance is not listed in the data sheet, but is probably on the order of 1 to 2 nHs.

## Model for Circuit Board Traces

Even the traces on circuit boards are not perfect. For our discussion, we will model the traces on the circuit boards as inductances.

## Output Noise

**Figure 6** shows a typical buck converter, with **Figure 7** showing some typical waveforms for that converter. The second graph from the bottom in Figure 7, labeled  $I(C_{OUT})$ , shows the current flowing into and out of the output capacitor. Note that the net DC current is zero (because it's a capacitor), but there is AC current flowing.

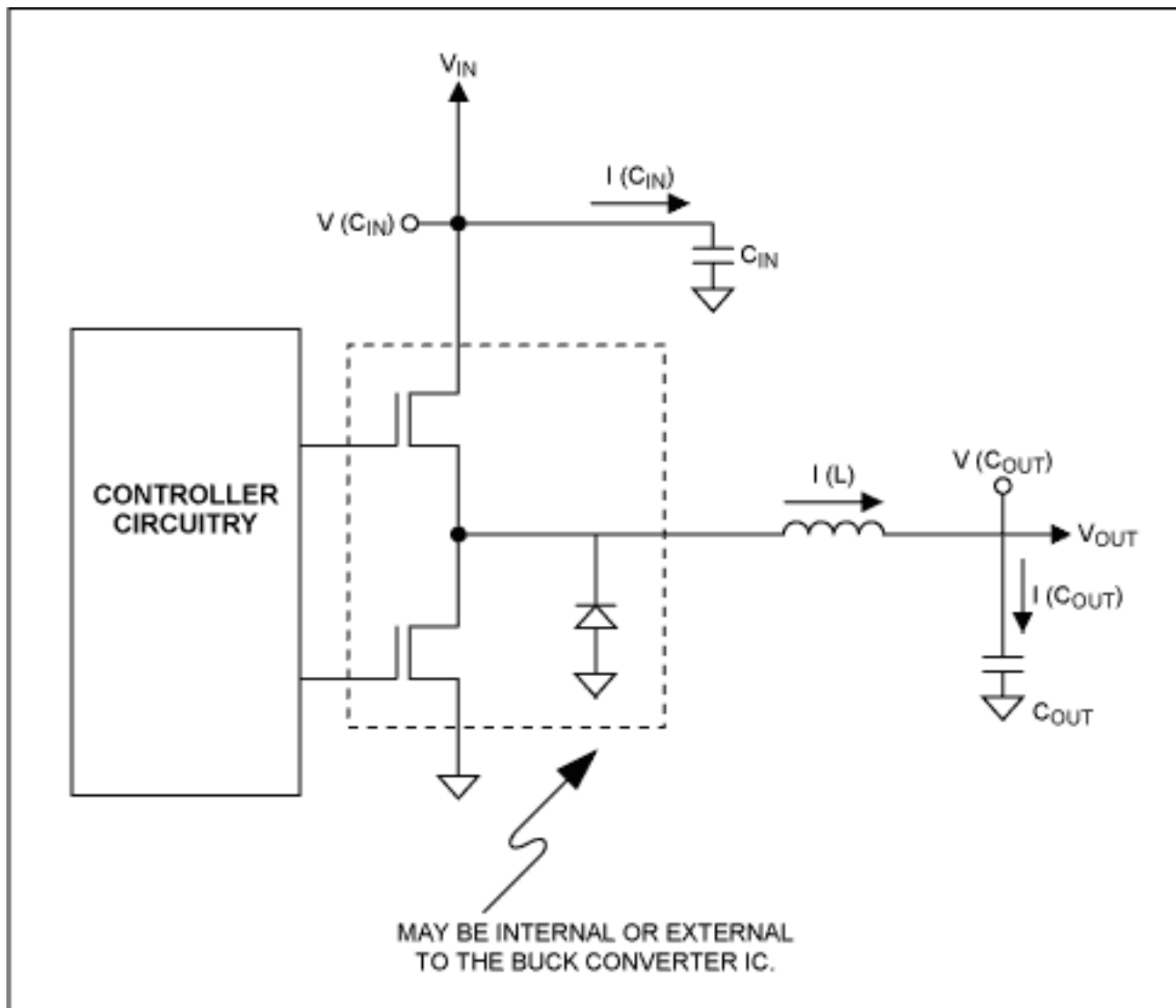


Figure 6. A typical buck converter circuit. Note that depending on the buck converter used, the low side MOSFET and or the catch diode may not be used.

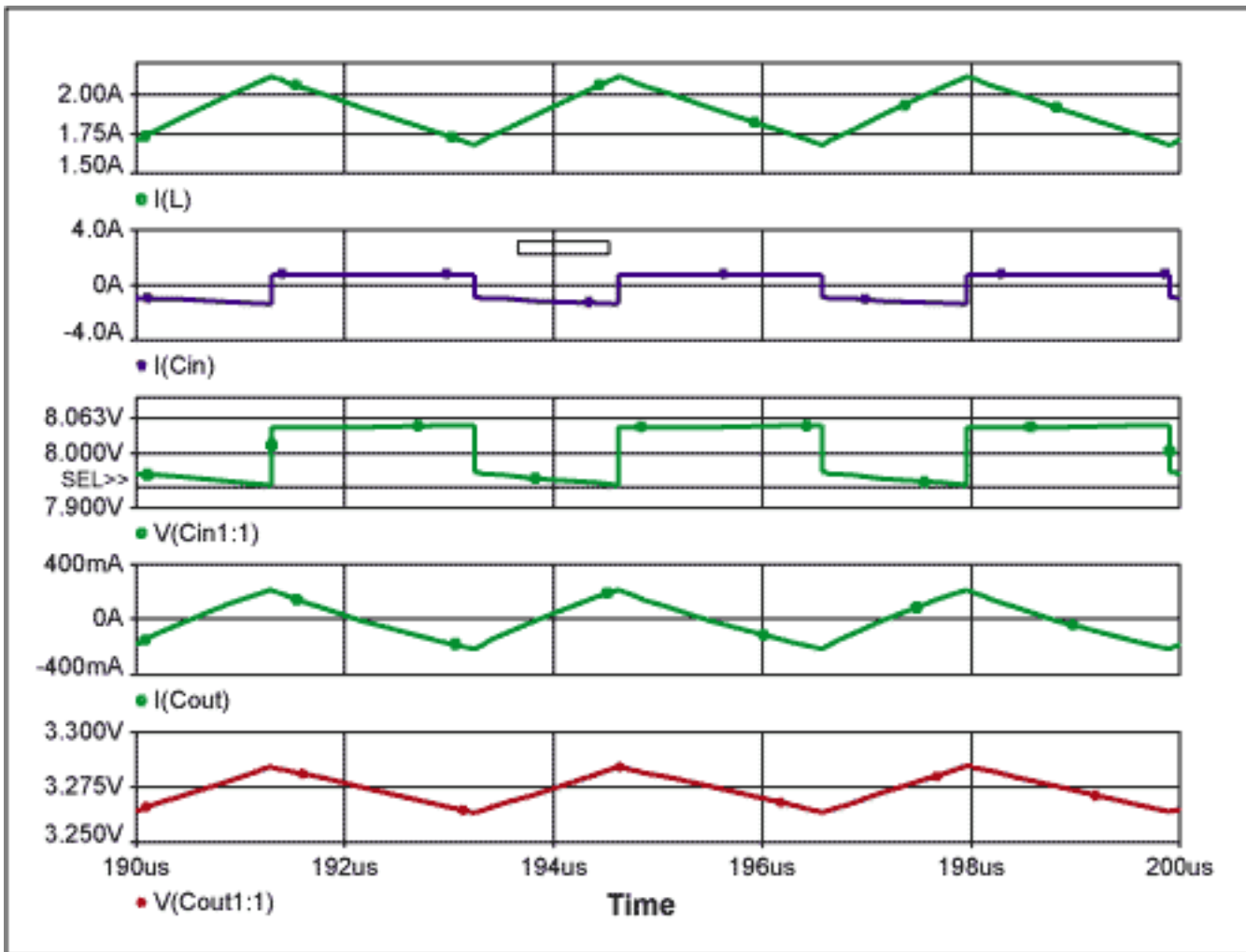


Figure 7. Shown are some typical waveforms for a buck converter. The top graph, labeled  $I(L)$ , shows the current waveform through the inductor. The next graph down, labeled  $I(Cin)$ , shows the current flow through the input capacitor. The third graph, labeled  $V(Cin1:1)$  shows the noise at the input of the converter that is due to the ESR of the input capacitor. The fourth graph, labeled,  $I(Cout)$  shows the current through the output capacitor. The bottom graph, labeled  $V(Cout:1)$ , shows the noise on the output of the converter, due to the ESR of the output capacitor.

This AC current working against the output capacitor's finite capacitance and ESR is what generates the output noise.

The first noise source we will discuss is finite output capacitance. Assuming for the moment that the output capacitor is ideal and that there is no ESR, the voltage on the capacitor is given by the age-old capacitor equation  $V = 1/C \int idt$ . With a little math, this formula has been changed to give Equation 2. Equation 2 calculates the peak-to-peak output noise due to this finite output capacitance. It is interesting to note that the output noise is independent of the load current.

$$V_{noise} = \frac{1}{8 \cdot f^2 \cdot L \cdot C_{out}} \cdot \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})$$

$V_{in}$  = the input voltage

$V_{out}$  = the output voltage

$f$  = the frequency at which the buck regulator is switching

$C_{out}$  = the capacitance of the output capacitor

L = the value of the inductor

$V_{noutc}$  = the peak-to-peak noise voltage due to the finite capacitance of the output capacitor

Equation 2. This equation calculates the peak-to-peak noise due to the finite capacitance of the output capacitor.

Figure 8 shows the output waveform measured using a MAX1653EVKit with high quality ceramic capacitors that have negligible ESR. The sin wave looking output ripple is due mostly to finite output capacitance.

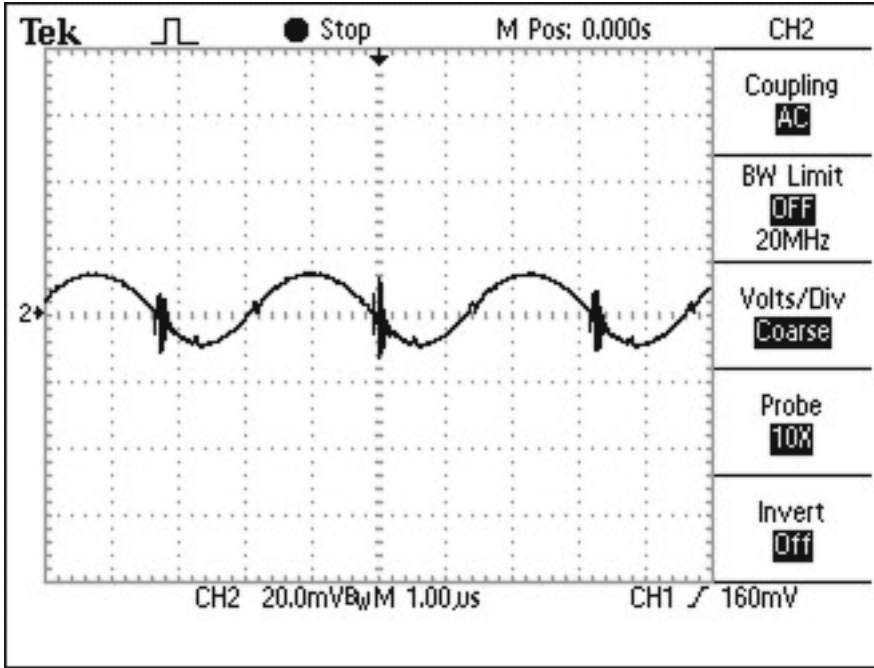


Figure 8. The noise on the output of a MAX1653EVKit, using 2 x 4.7µF ceramic capacitors. The measured peak-to-peak noise of 20mV agrees well with the calculated 18mV peak-to-peak.

Minimizing this source of noise is academically simple; just increase the value of the output capacitance. If there were no ESR, this would truly be the case. However, choosing a larger capacitor may, under some circumstances, actually increase the output noise if the ESR of the capacitor is larger.

## Output Capacitor ESR

The contribution to the noise due to the ESR of the output capacitor is easy to calculate. The peak-to-peak noise is given by  $V_{pp} = di \cdot R_{ESR}$ , where di is the peak-to-peak AC current going into the capacitor. Again, with a little mathematics, this equation can be expressed as shown in Equation 3. This equation gives the peak-to-peak noise due solely to the output capacitor's ESR.

$$V_{noutesr} = R_{coutesr} \cdot \left( \frac{1}{f \cdot L} \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out}) \right)$$

$V_{in}$  = the input voltage

$V_{out}$  = the output voltage

f = the frequency at which the buck regulator is switching

L = the value of the inductor

$R_{coutesr}$  = the ESR of the output capacitor

$V_{noutesr}$  = the peak-to-peak noise voltage due to the ESR of the output capacitor

Equation 3. Calculates the peak-to-peak output noise due to the ESR of the output capacitor.

The correct output capacitor choice is critical for a low noise design. The correct capacitor balances cost, low ESR and high capacitance.

## Input Noise

Many times engineers calculate the output noise, while ignoring the input noise. Buck converters will also cause conducted noise to be "injected" onto the input supply. For example, in the case of a 5V to 3.3V converter, the buck converter will cause noise on the 5V supply as well as generate noise on the 3.3V supply. If the 5V supply has noise sensitive components powered from it, this injected noise could be important. The section below describes what causes this noise. There are basically 3 major contributors: finite input capacitance, the input capacitor's ESR, and ringing that is caused by the stray inductance and stray capacitance in the circuit.

## Input Capacitor Capacitance

The current waveform that the input capacitor "sees" is shown in Figure 7, second graph from the top. This AC current works against the input capacitor's finite capacitance to create noise on the input supply. This noise is calculated in the same way as the noise on the output due to finite capacitance. Again, we use the capacitor equation  $V = 1/C \int i dt$ . Putting this equation into a form we can use yields the equations listed below in Equation 4. When making this calculation, be sure to include all the capacitances on the input supply, and not just the capacitance physically located next to the buck converter.

$$\frac{V_{out}^2}{2 \cdot f \cdot L \cdot V_{in} \cdot i_{out} - \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})} < 1$$

If this condition is met, use the equation below:

$$V_{nincin} = \frac{i_{out} \cdot V_{out} \cdot (V_{in} - V_{out})}{f \cdot C_{in} \cdot V_{in}^2}$$

$$\frac{V_{out}^2}{2 \cdot f \cdot L \cdot V_{in} \cdot i_{out} - \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})} > 1$$

If this condition is met, use the equation below:

$$V_{nincin} = \frac{1}{8 \cdot L} \cdot \frac{(V_{in} - V_{out})}{C_{in} \cdot V_{in}^2} \cdot \left( 2 \cdot L \cdot i_{out} + \frac{V_{out}}{f} \right)^2$$

$V_{in}$  = the input voltage

$V_{out}$  = the output voltage

$f$  = the frequency at which the buck regulator is switching

$L$  = the value of the inductor

$i_{out}$  = the output current

$V_{nincin}$  = the peak-to-peak noise voltage due to the finite capacitance of the input capacitor

$C_{in}$  = the capacitance of the input capacitor

*Equation 4. Gives the equations necessary to calculate the noise on the input supply voltage due to the input capacitor's finite capacitance.*

**Figure 9** shows a typical waveform of the noise due to finite input capacitance. This plot was taken with high quality ceramic capacitors that minimize any effect due to capacitor ESR. The large, high-frequency noise is unrelated to the finite input capacitance and is caused by the capacitors ESL. This is further discussed under the section labeled "Input Capacitors ESL".

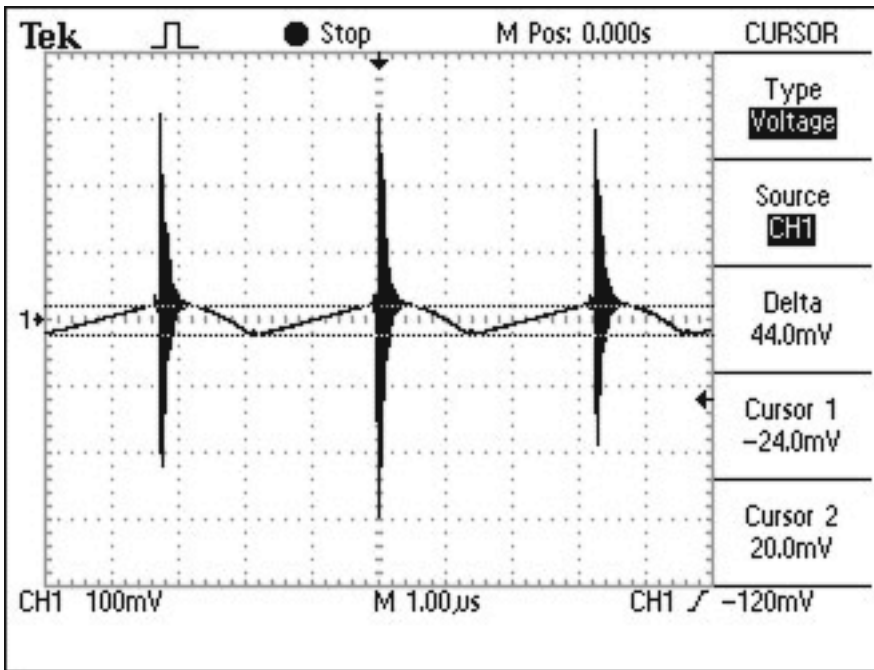


Figure 9. Shows a typical waveform of noise due to finite input capacitance.

## Input Capacitor ESR

The contribution to the noise by the ESR of the input capacitor is calculated using the same method that was used for the output capacitor. This peak-to-peak noise is given by  $V_{p-p} = di \cdot R_{ESR}$ , where  $di$  is the peak-to-peak AC current going into the capacitor. Equation 5 is the same basic formula, but in variables that are directly related to the circuit. **Figure 10** shows a typical waveform generated from an input capacitor's ESR. Again, the large high-frequency noise is due to the stray inductance and capacitance in the circuit and for the purposes of ESR noise should be ignored. This noise source is discussed next.

$$V_{n_{inesr}} = R_{c_{inesr}} \cdot \left( i_{out} + \frac{1}{2 \cdot f \cdot L} \cdot \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out}) \right)$$

$V_{in}$  = the input voltage

$V_{out}$  = the output voltage

$f$  = the frequency at which the buck regulator is switching

$L$  = the value of the inductor

$i_{out}$  = the DC output current

$R_{c_{inesr}}$  = the input capacitors ESR

$V_{n_{inesr}}$  = the peak-to-peak noise voltage due to the ESR of the input capacitor

Equation 5. Calculates the input noise due to the input capacitor's ESR.

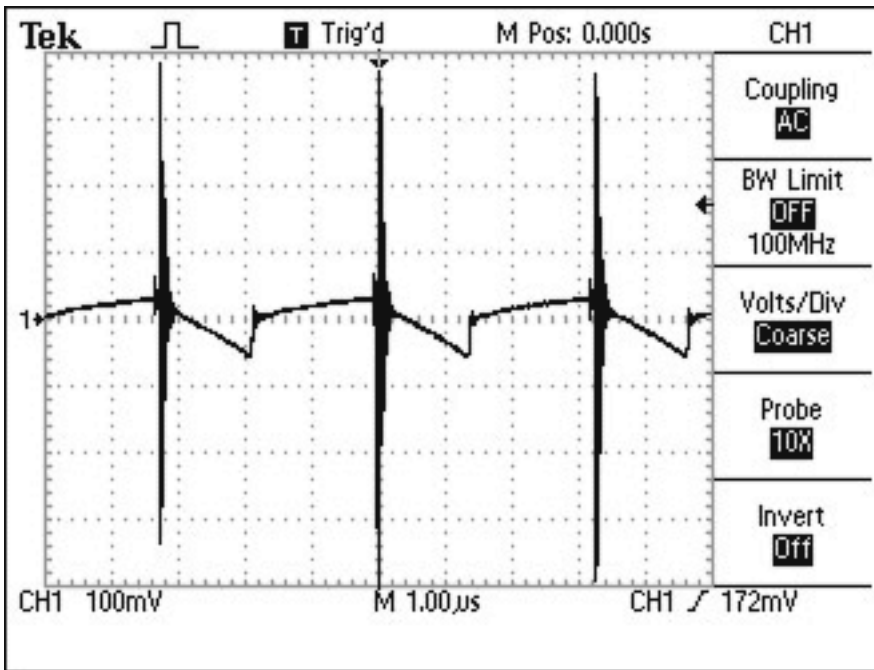


Figure 10. Shows the noise on the input due to the input capacitor's ESR.

## Input Capacitance ESL

Figure 10 shows the noise on the input of a MAX1653EVKit. Notice that there is some fast noise where the MOSFET switches. This noise is shown on an expanded time scale in **Figure 11**.

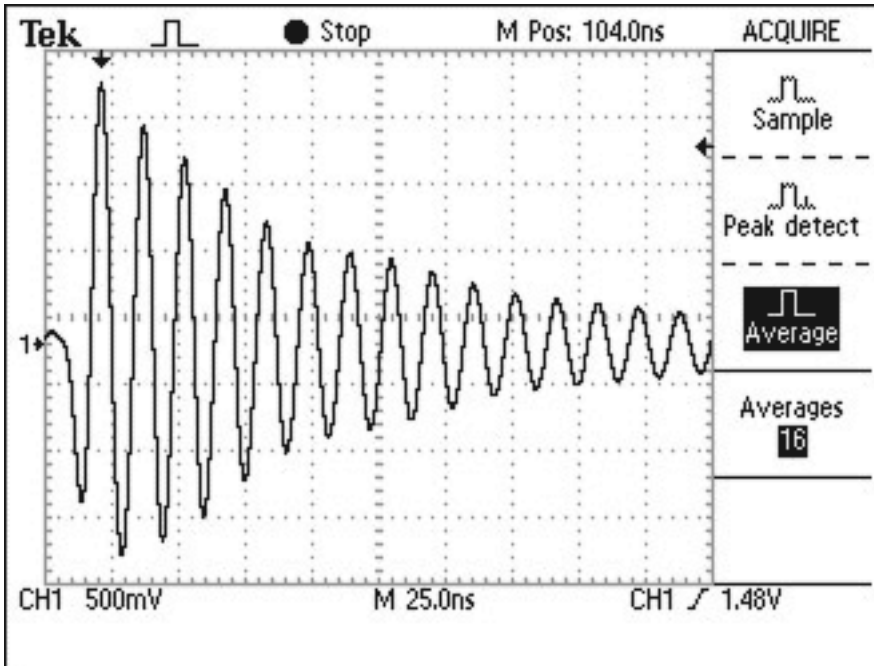


Figure 11. Shows an expanded view of the high-frequency noise on the input supply of a buck converter.

While the noise contributions due to the input capacitance and ESR are fairly intuitive, this noise source is much less obvious. Figure 6 shows a typical synchronous buck converter. We can redraw this buck converter to include all the non-ideal components as related to the MOSFETS, catch diode, input capacitor and traces as shown in **Figure 12**.

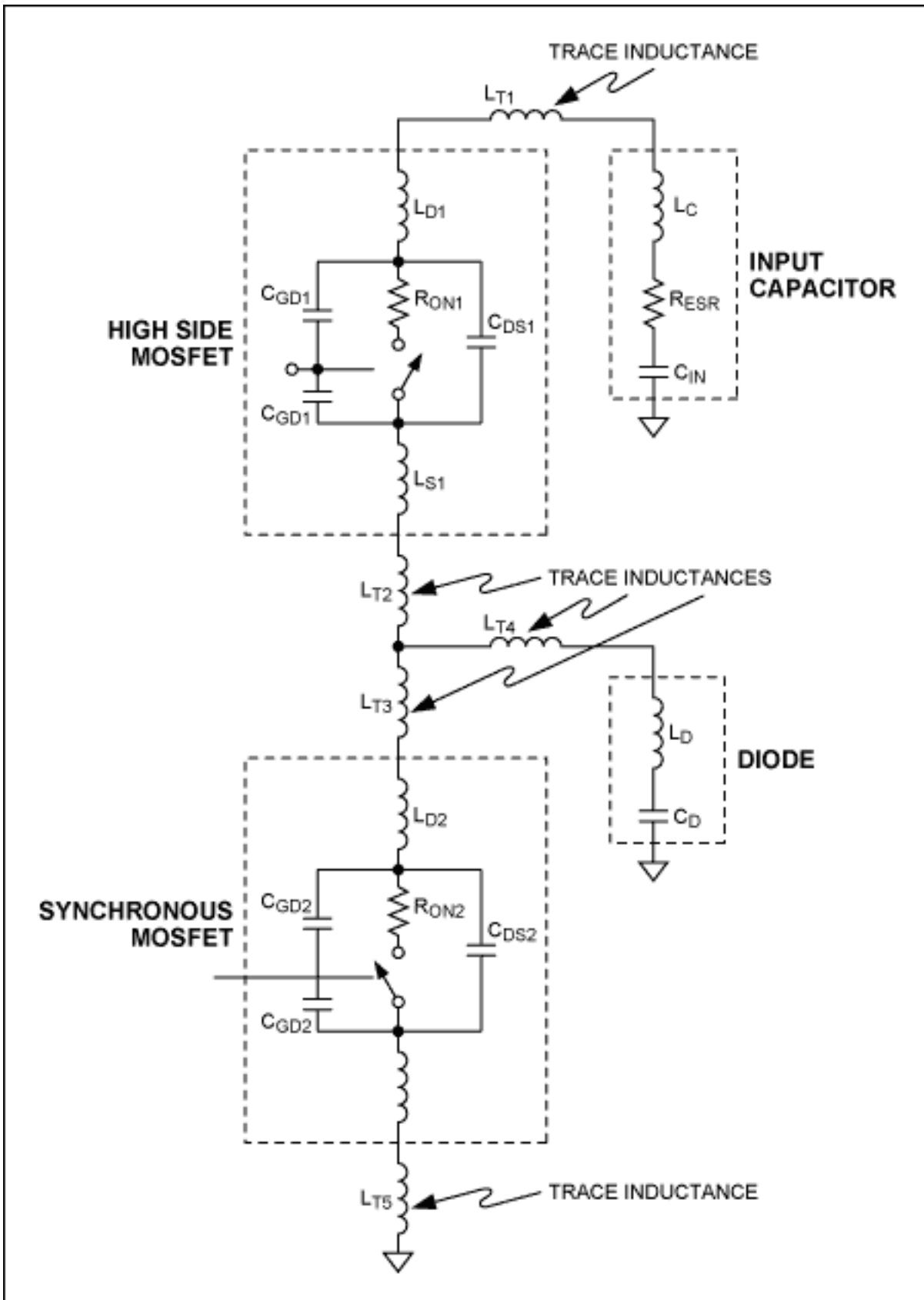


Figure 12. Shows the input side of a buck converter using the models developed earlier in this application note.

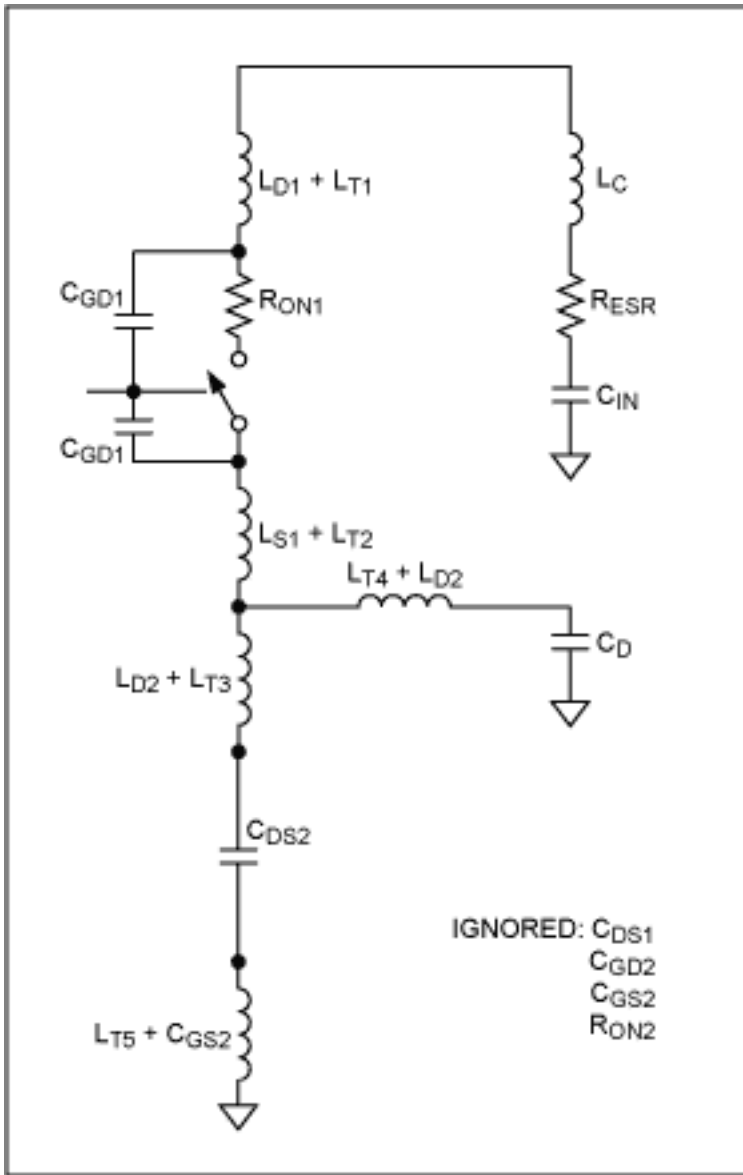


Figure 13. Shows a simplified version of Figure 12 where some components are combined, and trivial components are ignored.

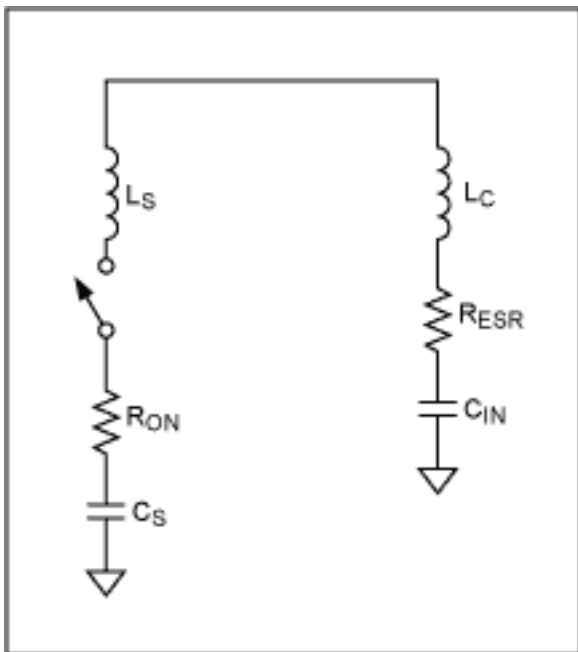


Figure 14. Shows a further simplification of Figure 12. Technical accuracy of this simplification was sacrificed for

simplicity.

Figure 12 can be simplified into Figure 13 by combining components and discarding parts that have negligible contributions. By taking some aggressive liberties, a further simplification of the circuit can be made to give Figure 14. While these aggressive liberties are not technically accurate, they are necessary to simplify understanding and to make the equations simpler. With our newly simplified circuit, it now becomes obvious that there is a series RLC tank circuit. When the switch closes, this tank circuit resonates in a classic manner. A series RLC circuit has a response as shown in **Figure 15**.

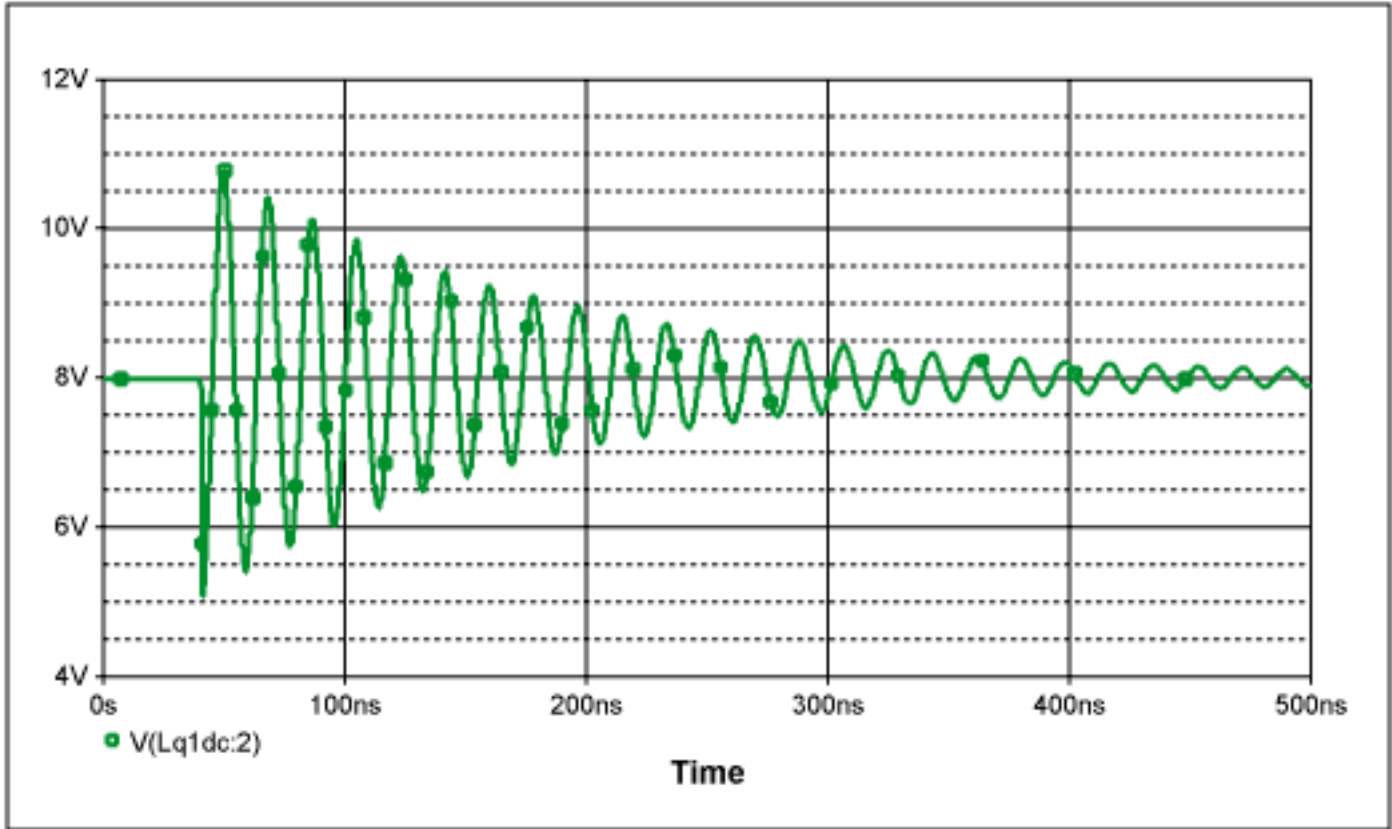


Figure 15. Shows the ideal waveform of Figure 14 when the switch is closed. This waveform assumes the input voltage (initial value of the capacitor) is 8V. The equations that govern this RLC circuit with respect to our simplified model are given below:

$$V_{pp} = \frac{L_s}{L_c + L_s} \cdot V_{in}$$

Equation 6. Gives the maximum peak to peak swing of an RLC series tank circuit as related to a buck converter.

$$\tau = 2 \cdot \frac{L_s + L_c}{R_{esr} + R_{on}}$$

Equation 7. Gives the decay constant for a classic RLC series circuit as related to a buck converter

$$f = \frac{1}{2 \cdot \pi \cdot \sqrt{(L_s + L_c) \cdot C_s}}$$

*Equation 8. Gives the ringing frequency of an RLC circuit as related to a buck converter.*

For the case where the buck converter uses an N-Channel MOSFET on the high side, the variables given in the above equations can be defined as below:

$V_{pp}$  = the maximum peak-to-peak noise voltage

$L_s = L_{t1} + L_{q1d} + L_{q1s} + L_{t2} + L_{t3} + L_{q2s} + L_{q2s} + L_{t4}$

$L_c$  = the equivalent series inductance of the input capacitor

$V_{in}$  = the input voltage

$\tau$  = the ring down time constant

$R_{esr}$  = the equivalent series resistance of the input capacitor

$R_{on}$  = the on-resistance of the high-side MOSFET

$C_s = C_{q2ds} + C_{q2gd}$

The case where a P-channel MOSFET is used on the high side is not as simple. When a N-channel is used, the capacitance of the high-side MOSFET can be ignored. This is because a floating gate driver is used, and basically shorts out most of the high-side MOSFET's capacitances. In the case of a P-channel, a floating gate driver is not used, and the capacitances cannot be ignored. Our aggressive oversimplification of the circuit is not as nearly as accurate in the case of a P-channel supply as it is for an N-channel supply. However, the basic concepts are the same, as are the solutions.

To check the relative accuracy of our simplified circuit in Figure 14, we can compare the response of the MAX1653EVKit shown in Figure 11 with that of the ideal waveform shown in Figure 15. The ideal waveform was generated using values obtained from the typical components used on the MAX1653EVKit. The MAX1653EVKit is ideal for comparison purposes, because it uses a high-side N-MOSFET.

The first thing that can be noticed is that the first low going cycle on the EVKit is not as big as that predicted by our simple model. The primary reason for this is the finite turn on time of the MOSFET. The MOSFET does not instantaneously go from high impedance to low impedance. This transition takes time. In the case of the MAX1653EVKit this transition is on the order of 5nS to 15nS. Because this transition time is roughly on the same order as the period of our ringing, the first cycle gets attenuated. This works in our favor to reduce the peak-to-peak noise. Other than the first low going cycle, our simplified model matches the lab results as well as can be expected.

Now that we understand the source of this ringing, how do we minimize it? Looking at Equation 6, we find that the noise is based on 3 variables: the input voltage (which we have little control over), the input capacitor's series inductance, and the sum of the inductances in the circuit. It becomes obvious (both mathematically and intuitively) to use input capacitors that have small series inductances. In addition, placing a small low inductance ceramic chip capacitor in parallel with the bulk capacitance can reduce the size of this noise. Keep these capacitors as close as possible to the MOSFETs (and/or catch diode). See **Figure 16**. A .01uF ceramic chip capacitor tends to be the sweet spot in terms of capacitance and low inductance. In addition to placing the .01uF capacitors at the input of the buck converter, placing these capacitors close to sensitive circuits that use the  $V_{in}$  supply will greatly reduce the noise at these circuits. One might also be tempted to reduce the slew rate of the gate drive to the MOSFET. Although this will reduce the noise, it could have negative effects on other aspects of the buck converter's performance, namely efficiency.

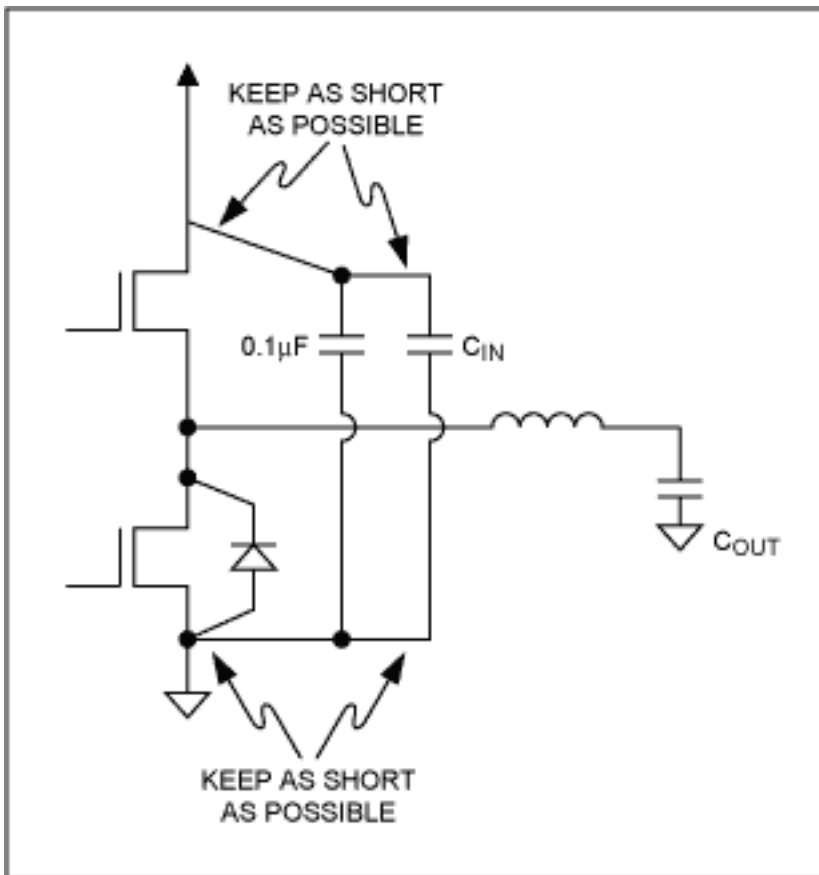


Figure 16. Placing a good ceramic chip  $.01\mu F$  capacitor in parallel with the bulk input capacitance, and placing both capacitors directly across the MOSFETs (or catch diode) will help minimize ringing on the input supply due to the bulk capacitor's ESL.

At this point it is appropriate to mention measuring techniques. Good measurement techniques are a good idea in general, but critical in trying to measure input capacitance ESL noise. When using a scope probe, keep the ground lead as short as possible. Connect both the signal portion of the probe and the ground lead directly across what you are trying to measure. Remember, this noise source is due to inductances on the order of nHs. It doesn't take much trace length to introduce nHs of inductance and ruin your measurement.

If further reduction of this noise source is necessary, a little input supply filtering can virtually eliminate the noise. The simplest/cheapest way is to separate the  $V_{IN}$  supply from the rest of your circuitry as much as possible. This adds a little inductance between the  $V_{IN}$  supply and the rest of the circuitry. This extra inductance provides some isolation effectively filtering this noise source. See **Figure 17**. Placing a small inductor in series with this supply line will virtually eliminate this noise source altogether. An inductor on the order of 200nH to 1uH is probably best. Too large of an inductor can have negative effects on circuit behavior. See **Figure 18**.

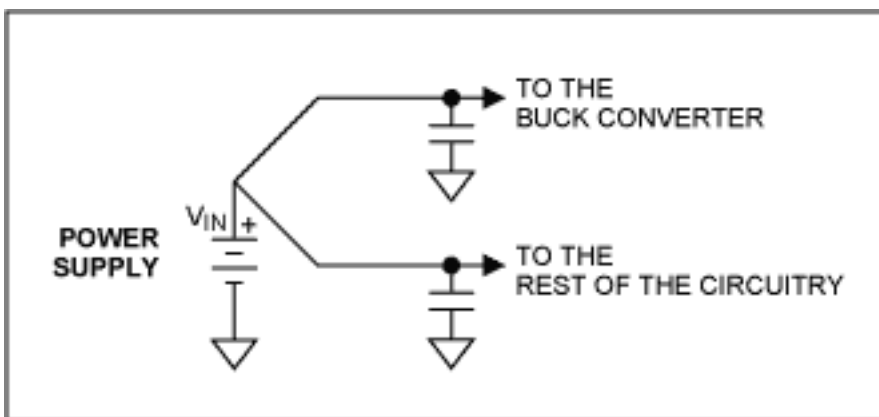


Figure 17. Separating the  $V_{IN}$  supply into 2 traces from the main power supply adds some trace inductance which acts to filter the noise caused by the input capacitor's ESL.

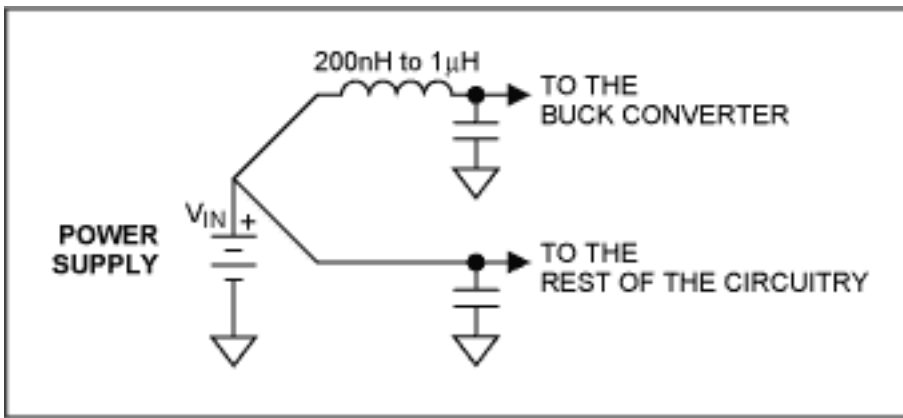


Figure 18. Adding a little inductance in series with the buck converter, will virtually eliminate the noise due to the ESL of the input capacitor.

## Summary of Equations

Noise due to finite capacitance	
Input Noise	$\frac{V_{out}^2}{2 \cdot f \cdot L \cdot V_{in} \cdot i_{out} - \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})} < 1$ <p>If this condition is met, use the equation below:</p> $V_{nincin} = \frac{i_{out} \cdot V_{out} \cdot (V_{in} - V_{out})}{f \cdot C_{in} \cdot V_{in}^2}$
	$\frac{V_{out}^2}{2 \cdot f \cdot L \cdot V_{in} \cdot i_{out} - \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})} > 1$ <p>If this condition is met, use the equation below:</p> $V_{nincin} = \frac{1}{8 \cdot L} \cdot \frac{(V_{in} - V_{out})}{C_{in} \cdot V_{in}^2} \cdot \left( 2 \cdot L \cdot i_{out} + \frac{V_{out}}{f} \right)^2$
Output Noise	$V_{noute} = \frac{1}{8 \cdot f^2 \cdot L \cdot C_{out}} \cdot \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out})$
Noise due to ESR of capacitor	
Input Noise	$V_{ninesr} = R_{cinesr} \cdot \left( i_{out} + \frac{1}{2 \cdot f \cdot L} \cdot \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out}) \right)$
Output Noise	$V_{noutesr} = R_{coutesr} \cdot \left( \frac{1}{f \cdot L} \cdot \frac{V_{out}}{V_{in}} \cdot (V_{in} - V_{out}) \right)$

$V_{in}$  = the input voltage

$V_{out}$  = the output voltage

$f$  = the frequency at which the buck regulator is switching

$C_{in}$  = the capacitance of the input capacitor

$C_{out}$  = the capacitance of the output capacitor

$L$  = the value of the inductor

$i_{out}$  = the output current

$R_{cinesr}$  = the input capacitors

$R_{coutesr}$  = the ESR of the output capacitor

$V_{noutesr}$  = the peak-to-peak noise voltage due to the ESR of the output capacitor

$V_{noutesr}$  = the peak-to-peak noise voltage due to the ESR of the output capacitor

$V_{noutc}$  = the peak-to-peak noise voltage due to the finite capacitance of the output capacitor

$V_{ninesr}$  = the peak-to-peak noise voltage due to the ESR of the input capacitor

$V_{nincin}$  = the peak-to-peak noise voltage due to the finite capacitance of the input capacitor

Note: The noise from the different sources are not in phase and therefore cannot be directly added.

---

Application Note 986: <http://www.maxim-ic.com/an986>

### **More Information**

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

Other questions and comments: <http://www.maxim-ic.com/contact>

AN986, AN 986, APP986, Appnote986, Appnote 986

Copyright © by Maxim Integrated Products

Additional legal notices: <http://www.maxim-ic.com/legal>