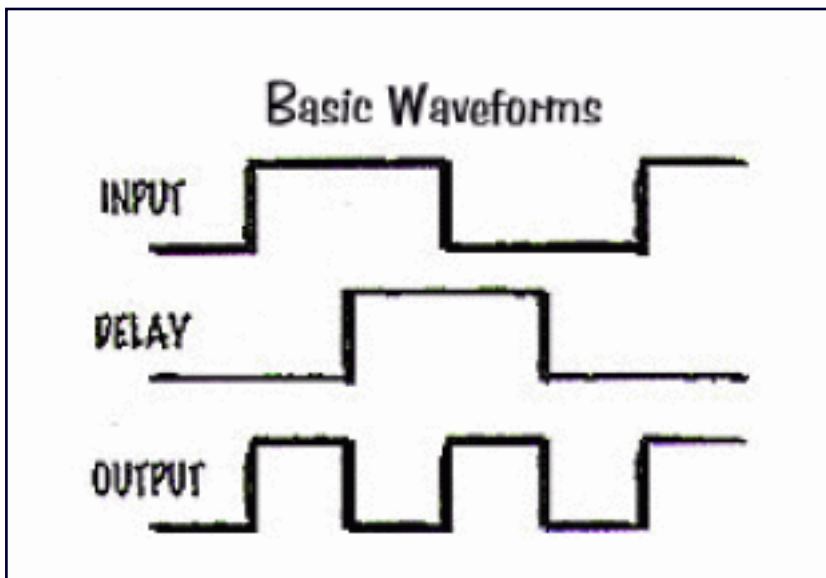
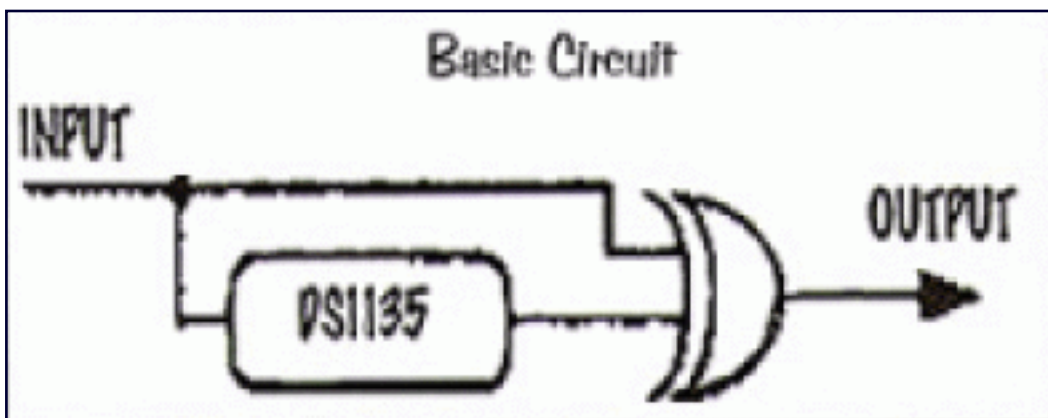


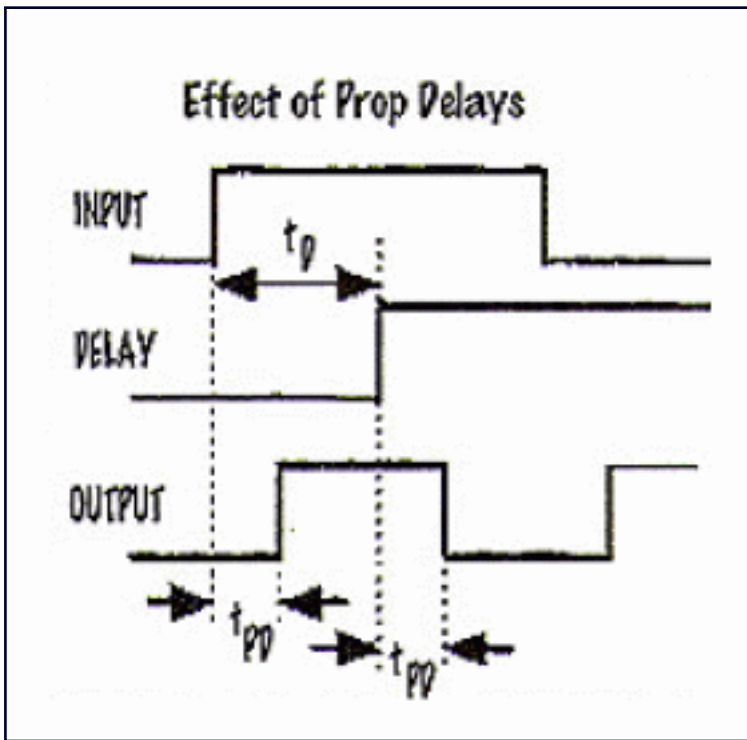
APPLICATION NOTE 881

Tech Brief 32: Frequency Doubler using Delay Lines

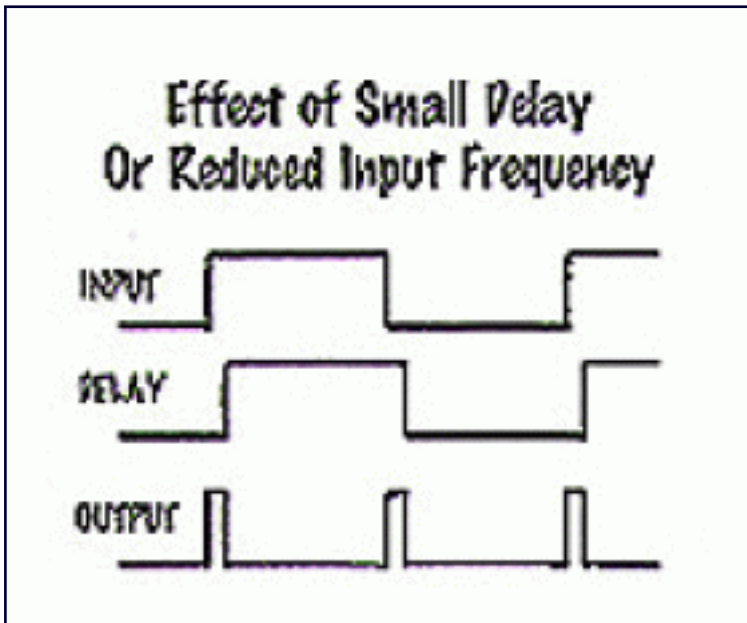
Abstract: Any independent delay line, in conjunction with a XOR gate, can be made into a clock frequency doubler by delaying the clock signal, and combining the delayed clock signal with the undelayed signal using the external logic. This application brief demonstrates how it can be done with a DS1035. The technique works with the DS1100 and DS1135 series as well.

If a clock signal is delayed by one-quarter period, it can be gated with the original waveform to produce a novel application: frequency-doubled output.

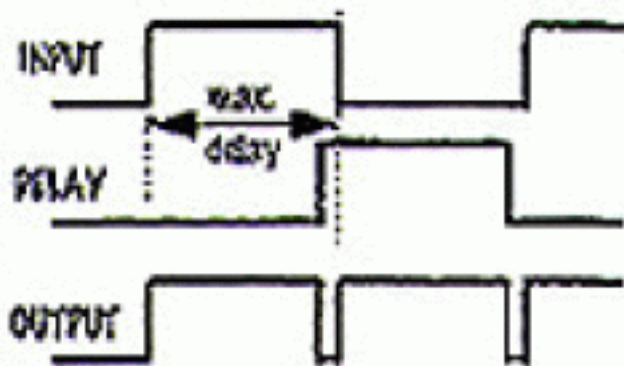




This time, the XOR propagation delay (t_{pD}) will impact only the relative skew from input to output and will not otherwise distort the waveform. Obviously, the optimum delay time for this application is one-quarter of the input period. Deviation from this "ideal" value, or altering the input frequency, will cause a change in the output duty cycle but will not change the frequency. The minimum usable delay (lowest usable input frequency) is dependent only on the minimum acceptable output pulse width or duty cycle. The maximum usable delay (highest input frequency) is constrained by the minimum input pulse width specification of the delay line.



Effect of large Delay Or increased Input Frequency



Application Note 881: <http://www.maxim-ic.com/an881>

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Related Parts

DS1004: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS1035: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

DS1100: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

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