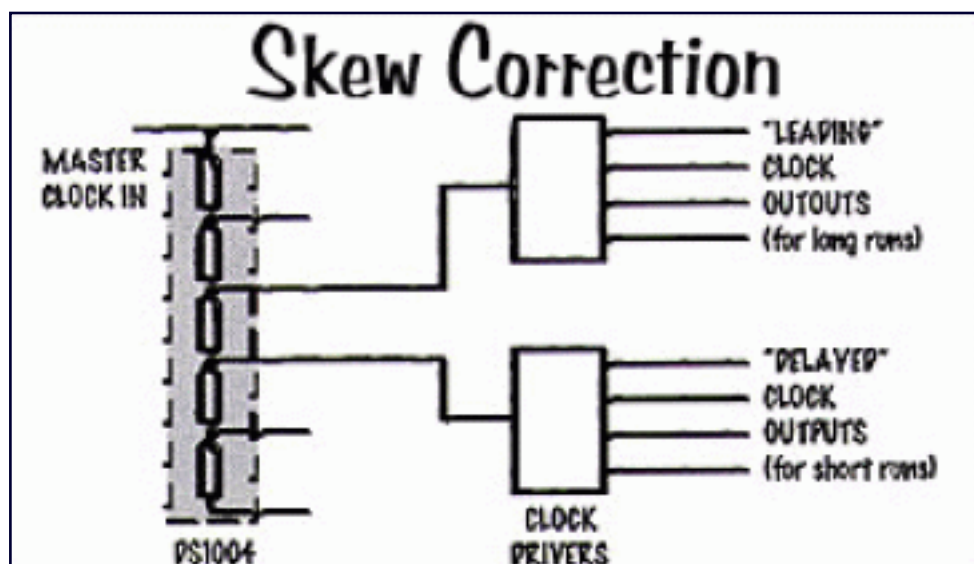


APPLICATION NOTE 879

Tech Brief 30: Skew Correction Using Delay Lines

Abstract: This application note describes using delay lines to correct system timing or "skew" of phased signals such as data and clock signals. Skew can be caused by signal delays in the signal path or inherent incompatibilities between system integrated circuits.

In systems with distributed clocks, great care is taken to ensure phase integrity through clock distribution trees. In cases where both long and short clock runs are needed, a similar configuration to the one above can be used to delay clocks taking short routes relative to those taking longer routes.



Note in this example that two successive tap outputs are used to feed the clock drivers, not the master clock and the first tap. This is because smaller delays are available tap-to-tap than from input to Tap 1, (e.g., down to 2ns for the DS1004). The smallest input to Tap 1 delay in the family is 4ns for the DS1100U-20, which may be too long unless very long runs are experienced.

Application Note 879: <http://www.maxim-ic.com/an879>

More Information

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