



APPLICATION NOTE 589

CPU Supervisors: Frequently Asked Questions

Abstract: This application note explains the function of a CPU supervisor and how it can monitor a system. The article discusses the function of a watchdog timer, chip-enable gating pin, and a sense input for an early warning signal. The document also focuses on the difference between a reset circuit and a voltage detector, and advises how to choose the proper voltage threshold.

What Is the Function of a Watchdog?

The watchdog timer allows the supervisor to monitor and restart a processor. In simplest terms, the watchdog timer restarts a clock each time that a transition occurs on its input. If the clock times out, then a reset or watchdog status output goes active. The input for the watchdog can be derived from many processor or system signals. Some of the most commonly used signals include data/address I/Os and interrupt outputs. In many cases a processor stalls because of a power transient, data, or software error. Monitoring processor operation can allow the supervisor to restart a stalled processor when no actual system problem exists. This capability saves some cost in system service personnel and can reduce downtime.

What Is the Difference Between a Reset and a Voltage Detector?

Voltage detectors simply indicate that a voltage is above or below a specific value. They do not provide any timing delays and generally have very limited noise immunity.

Resets provide a digital signal to the processor that not only indicates the voltage level, but also delays the reset signal so that the voltage can arrive at its nominal value. That delay also allows the power supply and board to fully stabilize prior to restarting operation.

What Device Reset Tolerance Should Be Used for Best Results?

Reset tolerance is a matter of personal preference as much as engineering necessity. Generally speaking, a device's reset tolerance should be set below the worst-case operation of the power supply. This means that a 5V power supply rated at $\pm 10\%$ would typically be used with a $5V \pm 10\%$ tolerance supervisor. Although a $\pm 5\%$ supervisor could be used in this application, spurious resets could be generated under normal operating conditions. Also, a $5V \pm 15\%$ supervisor might be used to allow for noisier power environments at the supervisor location, which are generally going to be worse than the conditions at the power supply output.

The operating voltages for system components can also be considered. However, because supervisors provide a delay on power-up, in many cases operating voltages are less critical when determining reset tolerance.

I Need a Dual 5V Reset. What Do You Have?

The [DS1834](#) device can have 5V applied to the 3.3V side to implement two resets with different trip points. If a resistor-divider is used, at least 10mA of current should be available to the input.

To What Does Device Tolerance Refer in CPU Supervisors?

Device tolerance can be used to refer to two different device values. One value is the voltage at which the device recognizes that power is good. On Maxim devices this value would generally be indicated simply as a percentage (for example, 5%). It would indicate that the device will trip just below the operating voltage minus 5%.

The other tolerance value is the variation or the accuracy of the trip point around its center point. In most cases this would be cited as plus-or-minus some percentage (e.g., $\pm 2\%$). Generally, most products supplied by Maxim operate with $\pm 2\%$ around the trip level or $\pm 2.5\%$ around the specified operating voltage.

What Is a Sense Input and NMI Output?

The (sense) input and NMI (non-maskable interrupt) output of referenced comparators are found on many CPU supervisor products. These functions can be configured to monitor an upstream voltage and thus provide an early warning of an impending power failure. This allows time to save critical data. In this application, the NMI output would generally be connected to a processor's NMI input. They also monitor secondary system voltages and provide a "system not ready" indicator to provide more consistent system operation. In this application, the NMI output can be connected to a processor interrupt, pushbutton reset input, or other control inputs.

What Are CEI and CEO Pins on Many of the CPU Supervisory Components?

A CEI (chip-enable input) and CEO (chip-enable output) provide a method to control RAM chip enable, based on the value of V_{CC} . The CEI is typically connected to a processor address output, RAM decode output, or directly to ground if the RAM is always enabled. The CEO is typically connected to the CE input on the RAM. This configuration allows the RAM to be automatically deselected if the voltage on V_{CC} is below the value rated to protect data during power transients. If not used, CEI would typically be connected to ground and CEO would be left floating.

Note: On devices with the prefix "MAX," CEI and CEO are labeled as CEIN and CEOUT.

What Is the Largest Capacitor Allowed for the Programmable Delay on Maxim CPU Supervisors?

The maximum capacitor size for the programmable delay is determined by the maximum leakage current. The larger the capacitor, the higher the capacitor quality needed to keep the leakage current below 1mA, otherwise the capacitor will never charge.

Can Active-Low RESET Remain Low Even When V_{CC} Falls Below the Minimum Operating Voltage?

On many parts active-low RESET can sink current even when V_{CC} is below the minimum operating voltage. The sink current falls dramatically once V_{CC} falls below $\sim 0.7V$ to $\sim 0.5V$.

What Is the Recommended Size of the Pullup Resistor for an Open-Drain, Active-Low RESET Output?

The resistor size depends on the application. Most applications can use a 10k Ω pullup resistor, although that value should be increased for applications requiring lower power dissipation.

What Supervisor Devices Does Maxim Offer?

Microprocessor supervisors come in many versions. Supervisors can monitor more than just one voltage, and have dual-/triple-/quad-/quint-voltage monitoring capabilities. Some supervisors are coupled with voltage-sequencing features to provide sequence timing as well as independent monitoring of each voltage. The latest microprocessor-supervisor devices can be found by visiting the [supervisors home page](#). Some devices and short descriptions are listed in **Table 1**.

Table 1. CPU Supervisors—Recent Product Releases

Supervisor	Description
MAX16016 , MAX16020 , MAX16021	Industry's most highly integrated microprocessor supervisor circuits provide battery backup and CE gating.
MAX16023 , MAX16024	Low-power battery-backup circuits with regulated output reduce the total number of external components.
DS3600	Secure supervisor with 64B nonimprinting, battery-backed, encryption key SRAM provides security, tamper detection, encryption key storage, and encryption key destruction in event of a tamper event.
DS3650	NV SRAM controller, RTC, and supervisor with tamper detection provides security, and encryption-key destruction in event of a tamper event.

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