

APPLICATION NOTE 5266

Quick Reference Guide for Programming the DS1877 SFP Controller

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Abstract: The DS1877 SFP controller allows various programming options to configure the alarms, warnings, lookup tables (LUTs), and other functions. This customization necessitates a large register memory map. This application note provides an alternate view of the register map, which is a helpful resource when programming the device.

Memory Map of the DS1877

The Main Device located at A2h is used for overall device configuration and transmitter 1 control, calibration, alarms, warnings, and monitoring. The transmitter 2 is controlled by the device located at address B2h.

- Lower Memory, A2h is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the Table Select byte.
- Table 01h, A2h primarily contains user EEPROM (with PW1 level access), as well as alarm and warning enable bytes.
- Table 02h, A2h/B2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers as well as other miscellaneous control bytes. All functions and status can be written and read from either A2h or B2h addresses.
- Table 04h, A2h contains a temperature indexed LUT for control of the MOD1 voltage. The MOD1 LUT can be programmed in 2°C increments over the 40°C to +102°C range.
- Table 05h, A2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h-FFh with the MASK bit enabled (Table 02h, Register 89h). In this case, Table 01h will be empty.
- Table 06h, A2h contains a temperature indexed LUT for control of the APC1 voltage. The APC1 LUT can be programmed in 2°C increments over the 40°C to +102°C range.

The Main Device located at B2h is used for transmitter 2 control, calibration, alarms, warnings, and monitoring.

- Lower Memory, B2h is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the Table Select byte.
- Table 01h, B2h contains alarm and warning enable bytes.
- Table 04h, B2h contains a temperature indexed LUT for control of the MOD2 voltage. The MOD2 LUT can be programmed in 2°C increments over the 40°C to +102°C range.
- Table 05h, B2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h-FFh with the MASK bit enabled (Table 02h, Register 89h). In this case Table 01h will be empty.
- Table 06h, B2h contains a temperature indexed LUT for control of the APC2 voltage. The APC2 LUT can be programmed in 2°C increments over the 40°C to +102°C range.
- Auxiliary memory (Device A0h) contains 256 bytes of EE memory accessible from address 00h-FFh. It is selected with the device address of A0h.

Refer to the tables below for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

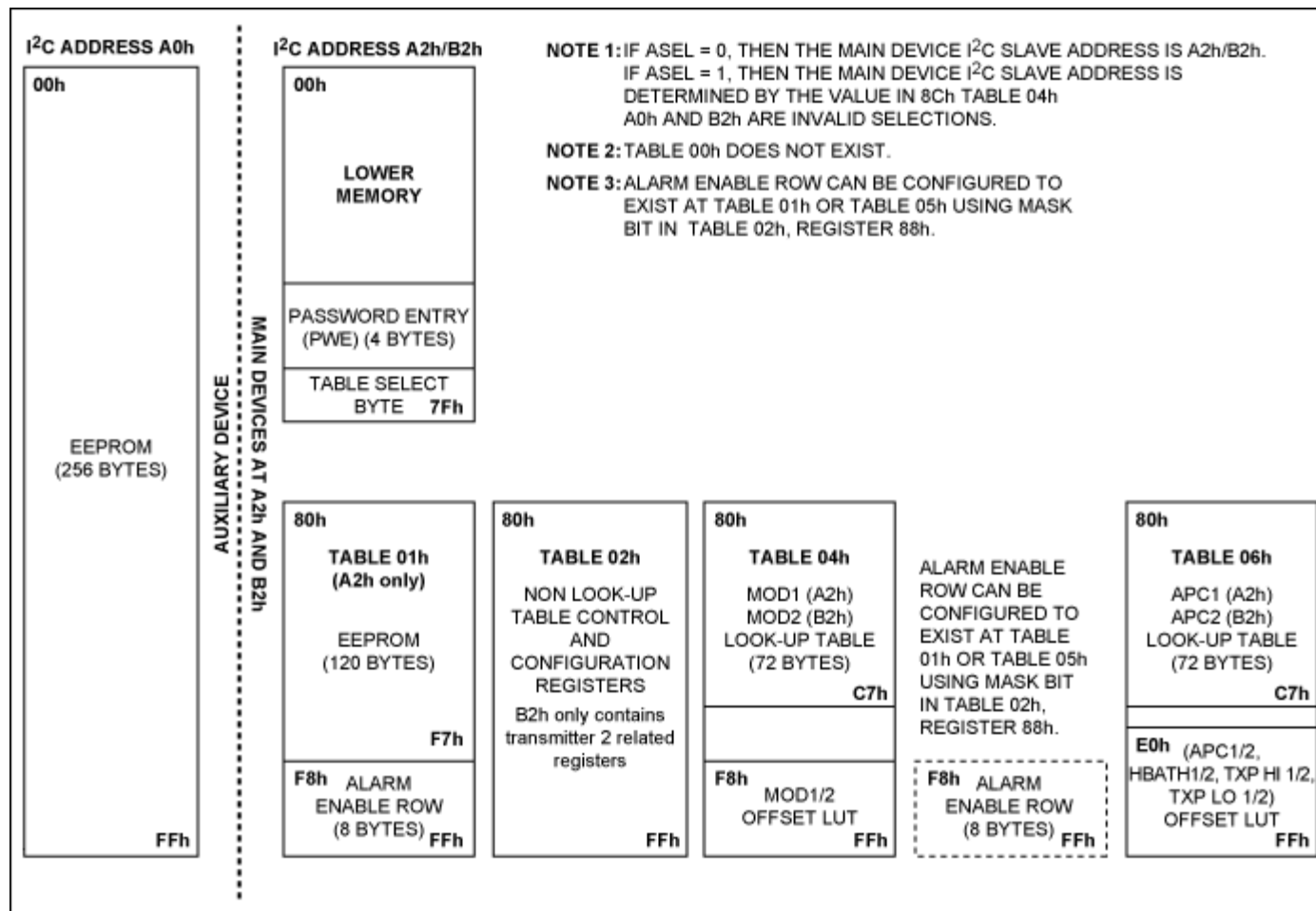
Shadowed EEPROM

Many nonvolatile (NV) memory locations (listed within the [Register Reference](#) section) are actually Shadowed EEPROM and are controlled by the SEEB bit in Table 02h, Register 80h.

The DS1877 incorporates Shadowed EEPROM memory locations for key memory addresses that may be written many times. By default, the Shadowed EEPROM Bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR} . Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value

written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. The memory map description indicates which locations are shadowed EEPROM.

DS1877 Memory Map



Register Reference

The following tables provide an easy reference to the Lower Memory, and Tables 00h, 01h and 02h. For description of the functionality for each bit, please refer to the corresponding register in the datasheet. Table 04h through 08h are Look-up tables that do not require a separate reference and hence are not included here. Please refer to the datasheet for detailed information about these tables.

The guide uses a color notation to distinguish between registers that can be accessed by the A2h and B2h memory. The notation is as follows:

	Memory Location is common to the A2h and B2h memory.
	Memory Location is different for the A2h and B2h memory.
	Register contains bits, some of which can be accessed only by the A2h memory, and some which can be accessed only by the B2h memory.

Note: RSVD is used as an acronym for reserved.

Lower Memory

Register Name	Register Addr (h)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEMP ALARM HI TEMP WARN HI	00, 04	S	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
	01, 05	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
TEMP ALARM LO TEMP WARN LO	02, 06	S	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
	03, 07	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
V _{CC} ALARM HI V _{CC} WARN HI	08, 0C	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	09, 0D	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
V _{CC} ALARM LO V _{CC} WARN LO	0A, 0E	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	0B, 0F	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
EE	10-1F	EE	EE	EE	EE	EE	EE	EE	EE
RSSI ALARM HI RSSI WARN HI	20, 24	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	21, 25	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RSSI ALARM LO RSSI WARN LO	22-26	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	23-27	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
PW2 EE	28-37	EE	EE	EE	EE	EE	EE	EE	EE
PW2 EE	38-4F	EE	EE	EE	EE	EE	EE	EE	EE
PW2 EE	50-5F	EE	EE	EE	EE	EE	EE	EE	EE
TEMP VALUE	60	S	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
	61	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
V _{CC} VALUE	62	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	63	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	64-67	0	0	0	0	0	0	0	0
RSSI VALUE	68	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	69	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	6A-6D	0	0	0	0	0	0	0	0
STATUS	6E	<5/D>RSVD	<5/D>TXDC	<2/C>INXS	<2/C>RSELS	<5/C>RSELC	<2/C>FLTS	<2/D>RXL	<2/C>RDYB
UPDATE	6F	TEMP RDY	V _{CC} RDY	RSVD	RSVD	RSSI RDY	RSVD	RSVD	RSSIR
ALARM ₃	70	TEMP HI	TEMP LO	V _{CC} HI	V _{CC} LO	RSVD	RSVD	RSVD	RSVD
ALARM ₂	71	RSSI HI	RSSI LO	RSVD	RSVD	RSVD	RSVD	RSVD	FLTINT
RESERVED	72	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
ALARM ₀	73	LOS HI	LOS LO	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
WARN ₃	74	TEMP HI	TEMP LO	V _{CC} HI	V _{CC} LO	RSVD	RSVD	RSVD	RSVD

RESERVED	75–7A	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
PASSWORD ENTRY	7B	2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴
	7C	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶
	7D	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	7E	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
TABLE SELECT	7F	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰

Table 01h

Register Name	Register Addr (h)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEPROM	80h–F7	EE	EE	EE	EE	EE	EE	EE	EE
ALARM EN ₃	F8	TEMP HI	TEMP LO	V _{CC} HI	V _{CC} LO	RSVD	RSVD	RSVD	RSVD
ALARM EN ₂	F9	RSSI HI	RSSI LO	RSVD	RSVD	RSVD	RSVD	RSVD	FLTINT
RESERVED	FA	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
ALARM EN ₀	FB	LOS HI	LOS LO	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
WARN EN ₃	FC	TEMP HI	TEMP LO	V _{CC} HI	V _{CC} LO	RSVD	RSVD	RSVD	RSVD
RESERVED	FD–FF	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Table 02h

Register Name	Register Addr (h)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MODE	80H	SEEB	DAC2 EN	RSVD	RSVD	AEN	DAC1 EN	RSVD	RSVD
T INDEX	81h	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	82–85	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
DEVICE ID	86	0	1	1	1	0	1	1	1
DEVICE VER	87	DEVICE VERSION							
CNFGA	88	RSVD	RSVD	RSVD	ASEL	MASK	INVRROUT	RSVD	INVLOSOUT
CNFGB	89	INXC	INVOUTX	ALATCH2	QLATCH2	WLATCH2	ALATCH1	QLATCH1	WLATCH1
CNFGC	8A	RSVD	TXD_RST EN DAC2	LOSC2	INVLOS2	RSVD	TXD_RST EN DAC1	LOSC1	INVLOS1
DEVICE ADDR	8B	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	8C	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
FORCE RSSI	8D	RSVD	XOVEREN2	RSSI2_FC	RSSI2_FF	RSVD	XOVEREN1	RSSI1_FC	RSSI1_FF
RIGHT SHIFT ₂	8E	RSVD	RSSI2C ₂	RSSI2C ₁	RSSI2C ₀	RSVD	RSSI2F ₂	RSSI2F ₁	RSSI2F ₀
RIGHT SHIFT ₁	8F	RSVD	RSSI1C ₂	RSSI1C ₁	RSSI1C ₀	RSVD	RSSI1F ₂	RSSI1F ₁	RSSI1F ₀
RESERVED	90–91	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
V _{CC} SCALE XOVER2 COARSE XOVER2 FINE	92, 94, 96, 98, 9A, 9C, 9E	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸

RSSI2 COARSE RSSI2 FINE RSSI1 COARSE RSSI1 FINE	93,95, 97, 99, 9B, 9D, 9F	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
INTERNAL TEMP OFFSET	A0	S	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²
	A1	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶
V _{CC} OFFSET XOVER1 COARSE XOVER1 FINE RSSI2 COARSE RSSI2 FINE RSSI1 COARSE RSSI1 FINE	A2, A4, A6, A8, AA, AC, AE	S	S	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰
	A3, A5, A7, A9, AB, AD, AF	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ⁴	2 ²³	2 ²²
PW1	B0	2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴
	B1	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶
	B2	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	B3	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
PW2	B4	2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴
	B5	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶
	B6	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
	B7	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
LOS RANGING ₂	B8	RSVD	HLOS ₂₂	HLOS ₂₁	HLOS ₂₀	RSVD	LLOS ₂₂	LLOS ₂₁	LLOS ₂₀
RESERVED	B9	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
HLOS ₂	BA	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
LLOS ₂	BB	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
LOS RANGING ₁	BC	RSVD	HLOS ₁₂	HLOS ₁₁	HLOS ₁₀	RSVD	LLOS ₁₂	LLOS ₁₁	LLOS ₁₀
RESERVED	BD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
HLOS ₁	BE	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
LLOS ₁	BF	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
PW_ENA	C0	RSVD	RWTBL1C	RWTBL2	RWTBL1A	RWTBL1B	WLOWER	WAUXA	WAUXB
PW_ENB	C1	RWTBL46	RTBL1C	RTBL2	RTBL1A	RTBL1B	WPW1	WAUXAU	WAUXBU
RESERVED	C2h–C5	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
POLARITY	C6	RSVD	RSVD	RSVD	RSVD	DAC2P	RSVD	DAC1P	RSVD
TBLSELPON	C7	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
DAC2 VALUE	C8	0	0	0	0	0	0	2 ⁹	2 ⁸
	C9	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	CA–CB	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

DAC1 VALUE	CC	0	0	0	0	0	0	2 ⁹	2 ⁸
	CD	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
RESERVED	CE–CF	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
EMPTY	D0–FF	EMPTY							

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