

Application Note:

HFAN-1.0.1

Rev 2; 04/08

Interfacing Single-Ended PECL to Differential PECL and Differential PECL to Single-Ended PECL



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1 Introduction

Although positive-referenced emitter-coupled logic (PECL) remains one of the standard logic families used for high-speed inputs and outputs in framer devices, the high current consumption of these outputs calls for an intermediate solution. Therefore, Maxim has released the MAX3881 and MAX3891 mux/demux chips, using single-ended PECL I/O for the parallel channels. When switching between single-ended and differential architectures, the unused inputs/outputs must be connected properly.

2 Interfacing Framer ICs with Differential PECL Outputs to the MAX3891

When interfacing the MAX3891 that has single-ended PECL inputs to a framer chip that has differential PECL outputs, the unused outputs from the framer must be terminated. Terminating the unused inverted outputs creates a more balanced load on the differential output, reducing output aberrations. The PCLKI inputs of the MAX3891 must be driven differentially. The MAX3891 uses an internal scheme similar to that shown in Figure 2 to determine the common-mode voltage of the PECL swings, which sets the vertical 0/1 threshold for the single-ended data inputs.

The most common interfacing scheme is shown in Figure 1. The pullup and pulldown resistors should be chosen so that they provide the Thévenin equivalent of 50Ω to $(V_{CC} - 2V)$. The following equation gives the proper conditions:

$$\text{Pullup} = \frac{50 \cdot V_{CC}}{(V_{CC} - 2V)} \quad \text{and}$$

$$\text{Pulldown} = 25 \cdot V_{CC}$$

For $V_{CC} = 3.3V$, pullup = 127Ω and pulldown = 82.5Ω . In order to minimize imbalance between the data lines, it is recommended that tight-tolerance 1% resistors be used.

The termination resistor on the unused (inverted) data outputs is chosen so that the unused PECL output sources approximately 14mA of DC current.

Typically, the common-mode voltage of PECL is $(V_{CC} - 1.3V)$. Therefore, in order to source 14mA:

$$\text{Termination} = \frac{V_{CC} - 1.3V}{14mA}$$

For $V_{CC} = 3.3V$, the termination resistor equals about 143Ω .

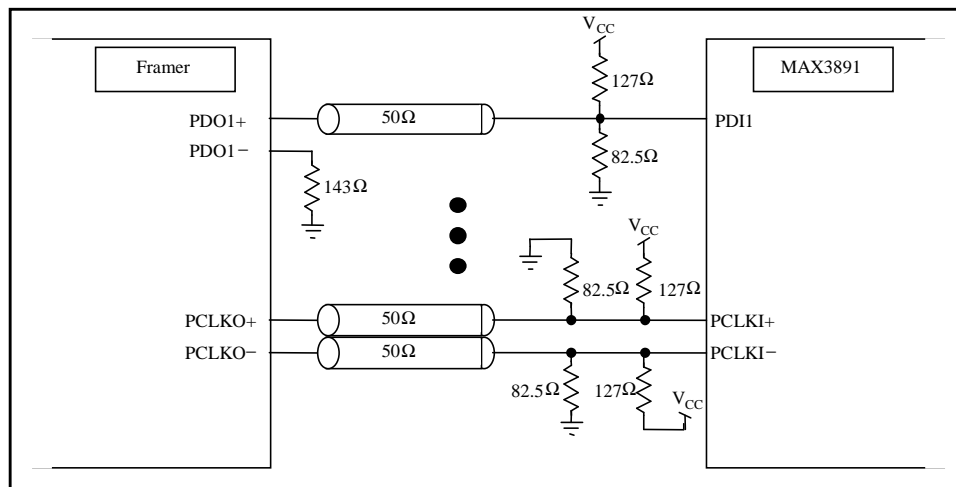


Figure 1. Connecting the MAX3891 to a differential PECL framer

3 Interfacing the MAX3881 to a Framer IC with Differential PECL Inputs

When interfacing the MAX3881 that has single-ended PECL outputs to a framer chip that has differential PECL inputs, the unused inputs of the framer IC must be driven to the common-mode voltage of the MAX3881 PECL output swing. This is because the framer determines '1's and '0's based on whether $IN+ > IN-$ (a '1') or $IN+ < IN-$ (a '0'). If the unused input, $IN-$, is not set to the proper level, errors can be induced.

The MAX3881 has differential PCLKO outputs. By using a circuit as shown in Figure 2, the common-

mode voltage of the PECL swings is determined and applied to the unused inputs. By employing this method, the common-mode voltage at the unused inputs is controlled carefully. Any changes in the common-mode voltage of PCLKO due to shifts in temperature and/or supply voltage can be tracked.

Again, the pullup and pulldown resistors set the Thévenin equivalent of 50Ω to $(V_{CC} - 2V)$. For $V_{CC} = 3.3V$, pullup = 127Ω and pulldown = 82.5Ω .

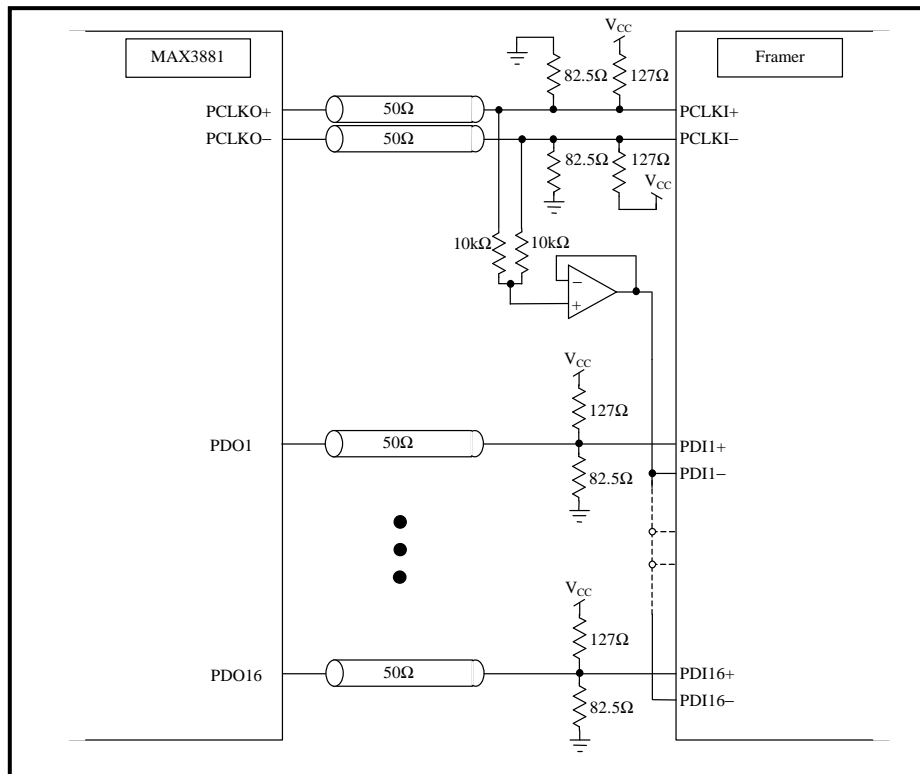


Figure 2. Setting the decision threshold using an adaptive amplifier

An alternative approach is to use a resistor voltage divider to generate the reference DC voltage, as shown in Figure 3. This method does not track the common-mode voltage of the PECL swings; therefore, the decision threshold will likely be shifted from its ideal voltage. A filter capacitor can

be included to minimize any noise due to crosstalk or feedthrough. This method can cause some pulse-width distortion in the recovered signal, which will increase the minimum setup and hold times for the input stage. The amount of setup and hold time margin lost will be discussed in the next section.

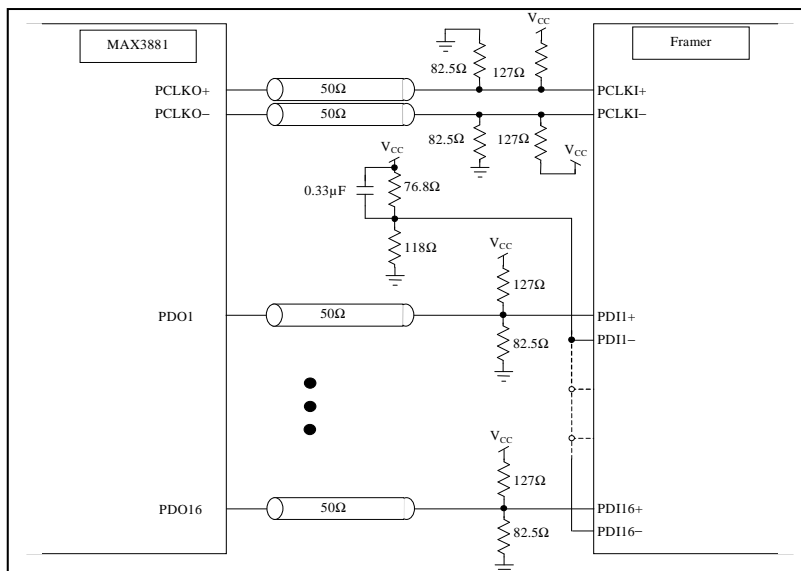


Figure 3. Setting the decision threshold using a supply referenced voltage divider

4 Calculating Pulse-Width Distortion (PWD) due to a Less-Than-Optimal Decision Threshold

When connecting the MAX3881 to a framer with differential inputs, if the unused inputs are not set to the proper DC level, then the input data appears to contain pulse-width distortion. This is because the unused input essentially sets the 0/1 decision threshold for the input stage. The problem is illustrated in Figure 4.

In order to avoid setup and hold time violations, the amount of PWD on the input signal must be calculated. Subsequently, the setup and hold times must be adjusted accordingly. We can assume that the worst-case rise and fall times for the PECL outputs of the MAX3881 is 1ns (20% to 80%). Because the minimum output swing is 530mV_{P-P}, we can approximate the worst-case slope at the crossing to be the following:

$$\frac{dV}{dt} = \frac{0.6 * 530\text{mV}}{1\text{ns}} = 318 \frac{\text{V}}{\mu\text{s}}$$

Now, if it is assumed that the maximum deviation of the common-mode voltage from (VCC – 1.3V) is ±150mV (a good assumption for the MAX3881), the maximum amount of pulse-width distortion on the signal can be found. This can be quantified as:

$$\begin{aligned} \Delta t &= \Delta V \left(\frac{dt}{dV} \right) = \Delta V \left(\frac{\mu\text{s}}{398 \text{ V}} \right) = \pm 150 \text{ mV} * \left(\frac{\mu\text{s}}{318 \text{ V}} \right) \\ &= \pm 472\text{ps} = \pm 0.073\text{UI} \end{aligned}$$

Thus, in order to avoid any possible setup and hold time violations, it is necessary to pad both the setup and hold times by 472ps.

Note that the above calculation uses worst-case conditions. Especially noteworthy is the assumption that the slope of the data crossing near the center of the eye is the 20% to 80% voltage swing divided by the 20% to 80% rise/fall time. Generally, the slope near the center of the data is much higher than near the top or the bottom, which will greatly reduce the pulse-width distortion due to voltage offsets.

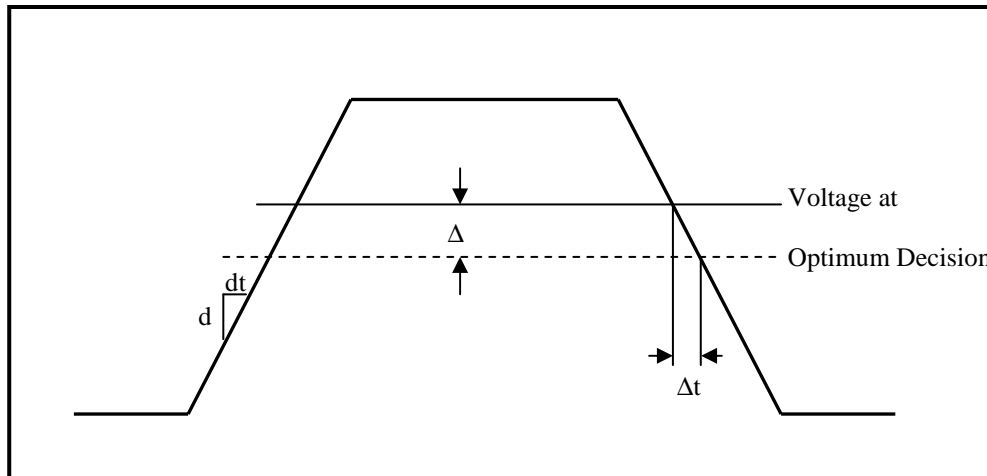


Figure 4. Calculating pulse-width distortion due to decision threshold offset