

Teridian 73S8024RN versus NXP TDA8024T

Introduction

This application note highlights the advantages of the Teridian 73S8024RN compared with the NXP Semiconductors TDA8024T Smart Card Interface IC.

The Teridian 73S8024RN is a single Smart Card Interface IC that provides all input and output signal interfaces as well as the power supply to the smart card. The Teridian 73S8024RN employs an on-chip LDO (Low Drop Out) regulator for the smart card power supply (V_{CC}). LDO regulators do not generate switching noise. This allows improved performance over devices that use DC/DC converter regulators. The Teridian 73S8024RN does require the analog power-supply input (V_{PC}) to be equal to 5 V typical (4.85V Min for NDS; 4.75V Min for EMV 4.0) to comply with applicable standards when using 5 V smart cards. The Teridian 73S8024RN LDO-regulator architecture also provides an overall solution that necessitates fewer components than the DC/DC converter solutions.

Package

The Teridian 73S8024RN IC is available in three different package options. The SO28 package is similar to the TDA8024T and is a direct drop-in replacement of the NXP part, taking into account the items listed in this document. The other two options are a 32QFN package (5 mm x 5 mm) and a 20QFN (4 mm x 4 mm), which allow dramatic reduction of the physical area used by the IC for space-limited PCB applications. Note the pin numbers mentioned in this document are references to the SO28 package.

Drop-in Replacement of the TDA8024T

In most of the existing applications that utilize a TDA8024T, the Teridian 73S8024RN can easily replace these parts. Particular attention to the three technical points detailed below will be sufficient, in most of the cases, to ensure a successful replacement. Refer to the next section of this document to learn more about the other technical differences that may marginally affect the behavior of the application.

Required Change

The 220 nF low ESR capacitor used with the TDA8024T that is located on the PCB close to the card connector (connected to the pin 17) is replaced by a 1 μ F low ESR cap when using the Teridian part in ISO7816 or NDS environments. Its placement should also be in close proximity to the card connector. Note that for EMV/non-NDS applications, a capacitor with a value of 3.3 μ F can give better LDO regulator stability when discharge time is not an important requirement.

Potential Cost Reduction Differences

The capacitor between pins 5 and 6 (the 100 nF low ESR charge pump capacitor of the TDA80x4 parts), and the capacitor connected to pin 8 (100 nF low ESR) can be removed.

The 100 nF capacitor between pins 17 and 14 is not necessary with the 73S8024RN and can be removed, however the 1 μ F capacitor should remain.

Note about the Use of the Pin 18 (SO28 Package)

Existing applications that utilize a TDA8024T may implement an optional resistor bridge connected to pin 18. This allows matching of the operating voltage range of the smart card interface IC (V_{DD} digital power supply IN) to the supply voltage range of the system controller. In other words, when the power supply of the system drops, the card interface is deactivated at the same time (or eventually before) the system controller. This feature is called in the *73S8024RN Data Sheet* “ V_{DD} Fault Adjust”.

To meet the exact voltage range (or V_{DD} fault value), the two resistor values must be slightly modified. Refer to the respective data sheets for exact calculation of these resistors. If leaving the NXP values, it will operate on a voltage range approximate to the NXP IC.

Advantages

1. **Improved Noise Performance.** The Teridian 73S8024RN Smart Card Interface chip uses a LDO regulator for the smart card power supply (V_{CC}), while the NXP TDA8024T device use a DC/DC converter which generates high levels of switching-noise. The advantages of the Teridian 73S8024RN can easily be seen when monitoring and comparing the noise on the ground (pins 4, 14, and 22) and supply (pins 6 and 21) pins against those of the NXP parts.

The comparisons shown below between the Teridian 73S8024RN and NXP TDA8024T were measured on the same reference PCB. The Teridian 73S8024RN had from two to four times less noise on the supply and ground pins. Table 1 shows the actual measurements and the oscilloscope pictures, on pages 3 and 4, clearly show the superior performance of the Teridian 73S8024RN IC.

Table 1: Noise Comparison

	LDO - 73S8024RN	DC/DC Converter – TDA8024T	Figure #
	Peak-to-Peak [mVpp]	Peak-to-Peak [mVpp]	
GND (Pin 4)	40	125	Fig. 1, 2
GND (Pin 14)	40	100	Fig. 3,4
GND (Pin 22)	45	125	Fig. 5,6
VPC/VDDp (Pin 6)	160	808	Fig. 7,8
VDD (Pin 21)	62	121	Fig. 9,10

Test Conditions

V_{PC}/V_{DDP} (Pin 6) = 5.0 [V]

V_{DD} (Pin 21) = 3.3 [V]

I_{CC} (@ V_{CC}) ~ 55 mA

T_a : Room temperature

All signals are measured with respect to a pre-defined reference point (GND on test PCB).

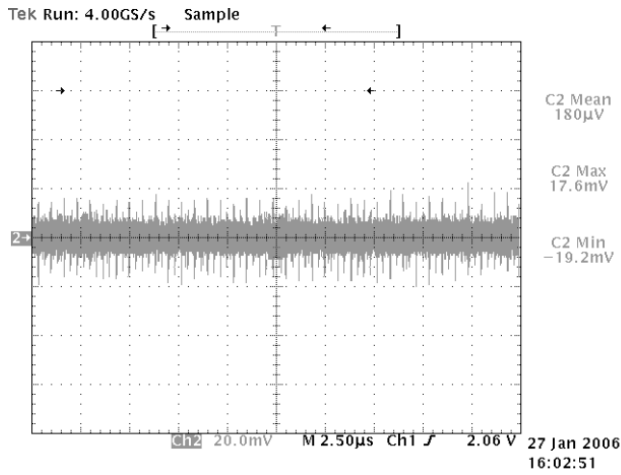


Figure 1: Teridian 73S8024RN, GND (Pin 4)

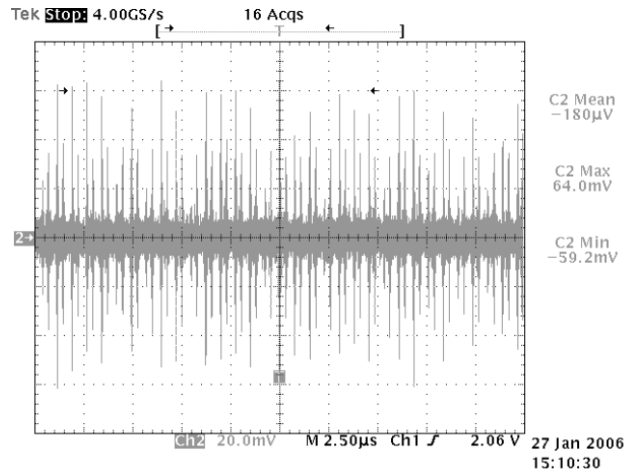


Figure 2: NXP TDA8024T, GND (Pin 4)

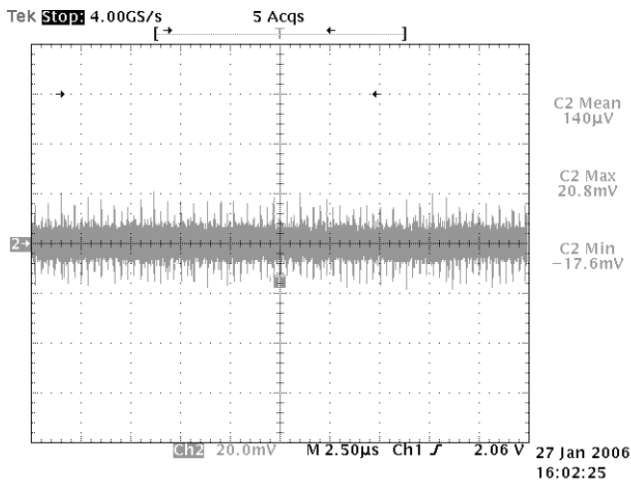


Figure 3: Teridian 73S8024RN, GND (Pin 14)

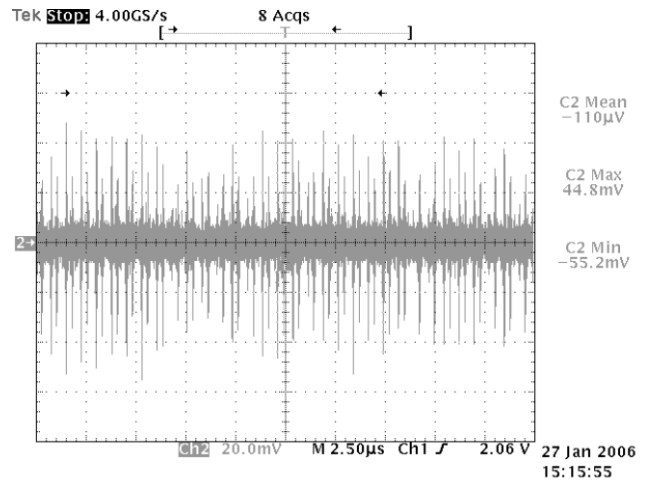


Figure 4: NXP TDA8024T, GND (Pin 14)

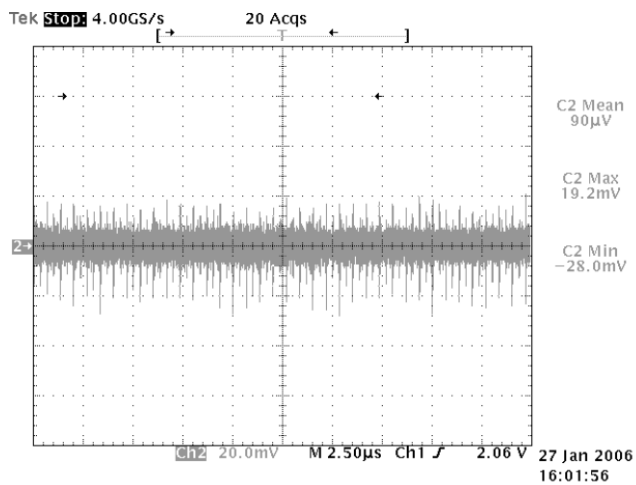


Figure 5: Teridian 73S8024RN, GND (Pin 22)

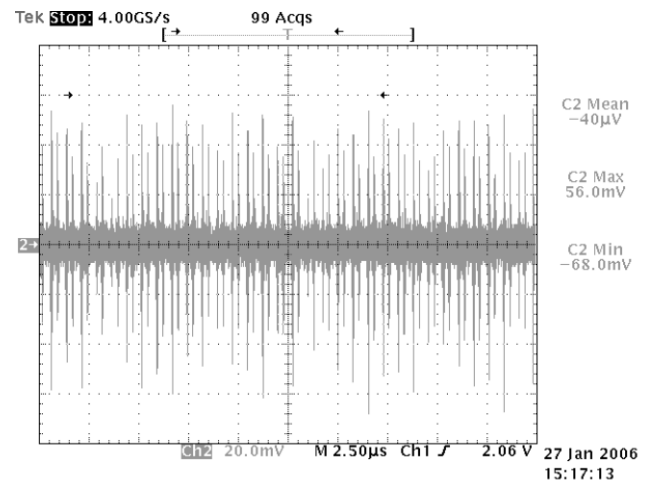


Figure 6: NXP TDA8024T, GND (Pin 22)

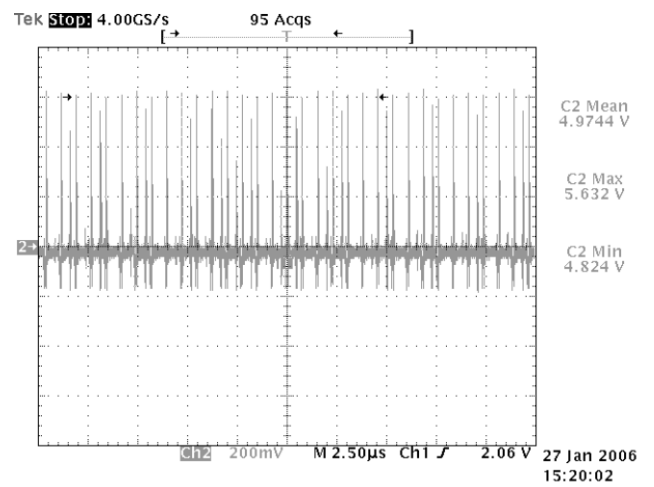
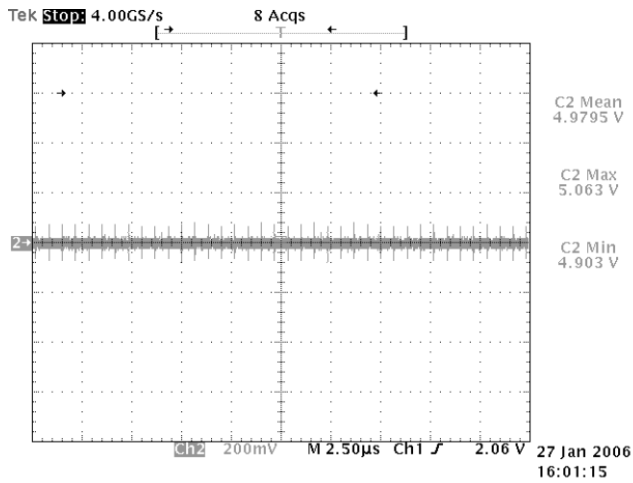


Figure 7: 73S8024RN V_{PC} , Regulator Supply (Pin 6) Figure 8: TDA8024T V_{DDP} , DC/DC Converter Power Supply (Pin 6)

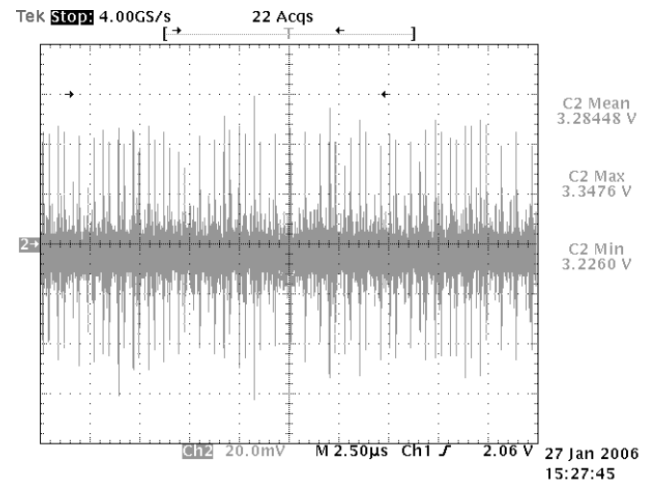
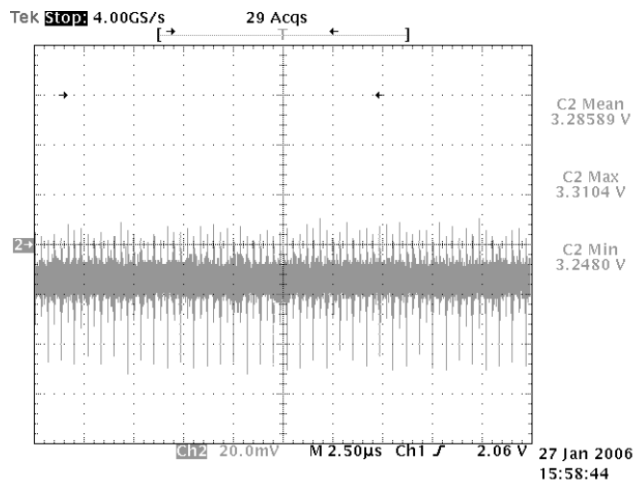
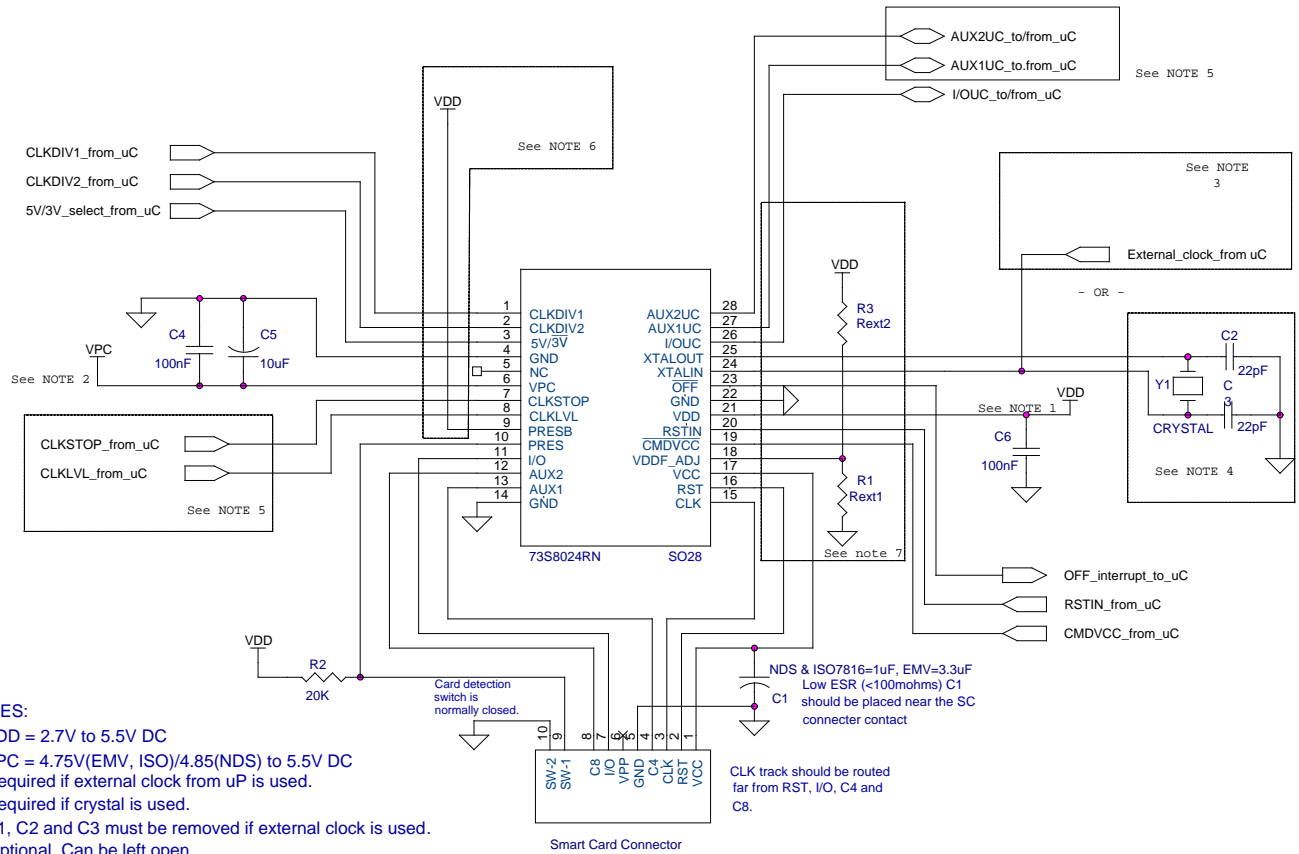


Figure 9: 73S8024RN V_{DD} Digital Power Supply (Pin 21) Figure 10: TDA8024T, V_{DD} Digital Power Supply (Pin 21)

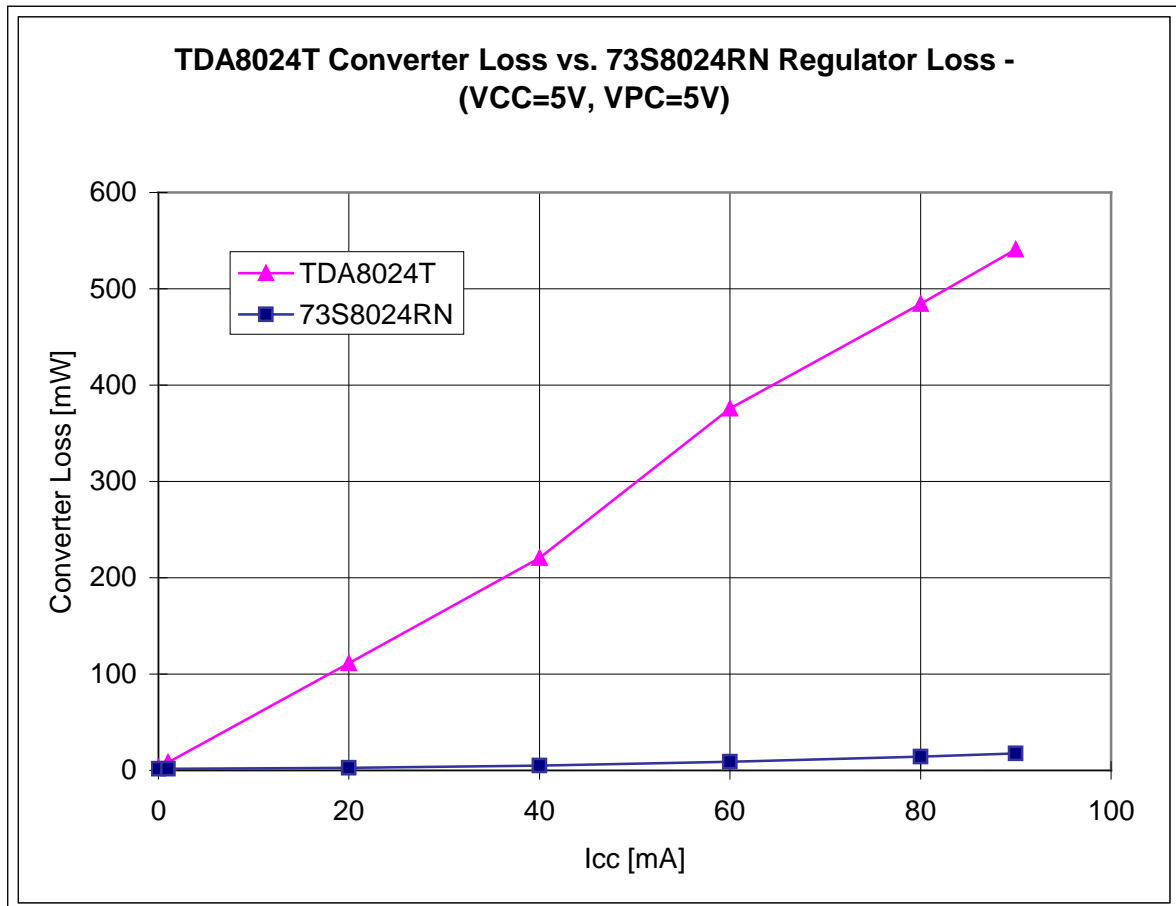


NOTES:

- 1) VDD = 2.7V to 5.5V DC
- 2) VPC = 4.75V(EMV, ISO)/4.85(NDS) to 5.5V DC
- 3) Required if external clock from uP is used.
- 4) Required if crystal is used.
Y1, C2 and C3 must be removed if external clock is used.
- 5) Optional. Can be left open.
- 6) Internal pull-up allows it to be left open if unused.
- 7) R1 and R3 are external resistors that adjust the VDD fault voltage. Can be left open.

Figure 11: Teridian 73S8024RN Application Schematic

2. **Improved Card Power Supply Efficiency.** The following graph shows the difference between the TDA8024T converter loss and the 73S8024RN regulator loss. It is obvious that the 73S8024RN is much more efficient than the TDA8024T over the load range.



3. **3 Volt Only Operation.** The Teridian 73S8024RN Smart Card Interface IC allows true 3.3 V only operation when used with 3 V smart cards. Setting the 5V/3V pin low (pin 3 on the SO28 package, pin 31 on 32QFN package), sets the Teridian 73S8024RN to true 3.3 V only operation. This allows the elimination of the 5 V supply in many Set Top Box (STB) applications. The NXP TDA8024T must always supply 5 V to the DC/DC converter and thus cannot operate as a true 3.3 V only device.
4. **PCB Space and BOM Cost Reduction.** The Teridian 73S8024RN IC requires fewer external components than the NXP TDA8024T. With the Teridian 73S8024RN, three low-ESR capacitors can be eliminated from the BOM. The Teridian 73S8024RN only requires one filter capacitor at the smart card supply voltage pin (V_{CC}), whereas the NXP TDA8024T requires two. Also, with the LDO regulator, the Teridian 73S8024RN eliminates the two capacitors that are needed for the DC/DC converter.

The Teridian 73S8024RN comes in a SO28 package. With this package option, it is pin compatible to the NXP TDA8024T. The Teridian 73S8024RN also comes in a 32QFN (5mm x 5mm) and 20QFN (4x4mm) packages allowing for a more compact, space saving PCB design.

5. Feature Enhancements.

a. Smart Card Power Down Mode

The Teridian 73S8024RN has a smart card power-down mode, by performing a Clock Stop on the smart card clock signal (CLK). Pins 7 and 8 of the SO28 package that are normally used to connect the DC/DC converter capacitor in the NXP TDA8024T parts, are used for the digital inputs CKSTOP and CKLEV. These allow the host to stop the clock to the smart card, in either a High (CKLEV=1) or Low (CKLEV=0) voltage state. This mode is a power saving mode not supported by the NXP devices. These pins can be left unconnected if this Card Power Down Mode is not required.

b. Adjustment of the V_{DD} Fault Threshold Voltage

By default, the Teridian 73S8024RN, in common with the NXP TDA8024T, begins an automatic deactivation sequence of the smart card when the digital power supply (V_{DD}) drops below a threshold value. This value is trimmed at the factory to be $2.3V \pm 0.1 V$. In some applications, it might be desirable to have a different voltage threshold (to deactivate the card earlier for instance). The Teridian 73S8024RN provides the option to modify this threshold value by connecting an external resistor to the V_{DDF_ADJ} pin. Either a single resistor from the V_{DDF_ADJ} pin to ground or two resistors, one from the V_{DDF_ADJ} pin to ground and the other from V_{DDF_ADJ} to V_{DD} , can be used to adjust the V_{DD} fault level. This single resistor option is simpler, but the trigger threshold is less accurate. The two resistor option is much more accurate. Refer to the Teridian *73S8024RN Data Sheet* for further detail. This feature is supported by the TDA8024T, but requires different resistor value(s) for the same threshold voltage. When unused, pin 18 on the Teridian 73S8024RN must be left unconnected.

c. Sequencer (Activation)

Unlike the TDA8024T, the Teridian 73S8024RN IC internally generates the EMV 4.0 compliant CLK to RST delay at activation. The related timing differences between 73S8024RN and TDA8024T are:

- With the 73S8024RN, the CLK doesn't start unless RSTIN goes low. There is no timeout for this event. In this manner, the host processor easily controls the CLK start. The TDA8024T has a small window between 50 and 220 μs where the falling edge of RSTIN can start CLK. After 220 μs the CLK will start regardless of the state of RSTIN.
- 73S8024RN automatically asserts 42,000 CLK cycles of RST delay at activation. Negative pulse width on RSTIN can be shorter than this delay. The TDA8024T doesn't provide any delay; RST is active immediately after the CLK starts.
- Activation is invoked by negating \overline{CMDVCC} . CLK start timing depends on RSTIN fall timing. Three cases for CLK starts are illustrated in Figure 12.
- Case 1: RSTIN goes low when $t < T_0$
 73S8024RN – CLK starts at T_1 (approximately 600 μs after \overline{CMDVCC} goes low).
 TDA8024T – CLK starts between 50.2 and 130.2 μs .
- Case 2: RSTIN goes low when $T_0 < t < T_1$
 73S8024RN – CLK starts at T_1 . If RSTIN is de-asserted (rises) before T_1 , it is ignored and CLK and I/O stay low until next RSTIN de-assertion (same as case 3).
 TDA8024T – As mentioned above, there is a window between 50 and 220 μs where the falling edge of RSTIN can start CLK.
- Case 3: RSTIN goes low when $t > T_1$
 73S8024RN – CLK starts at RSTIN fall timing.
 TDA8024T – CLK starts 220 μs from falling edge of \overline{CMDVCC} .

RST de-assertion (RST rising)

73S8024RN - RST is de-asserted at 42,000 CLK cycles (T_2) after CLK start if RSTIN becomes high before T_2 (A). If RSTIN goes high after T_2 , RST is de-asserted at RSTIN rising as demonstrated in (B). In this manner, the 42,000 clock-cycle delay, as per EMV 4.0 and ISO7816-3 is ensured by the 73S8024RN, and longer delay can also be CLK to RST delay can be controlled by the system controller.

TDA8024T – After CLK has started, RST will track RSTIN.



The 73S8024RN activation sequence and its controlling host firmware are fully compatible with the TDA8024T (as long as the RSTIN line is asserted and de-asserted by the host after time T_2).

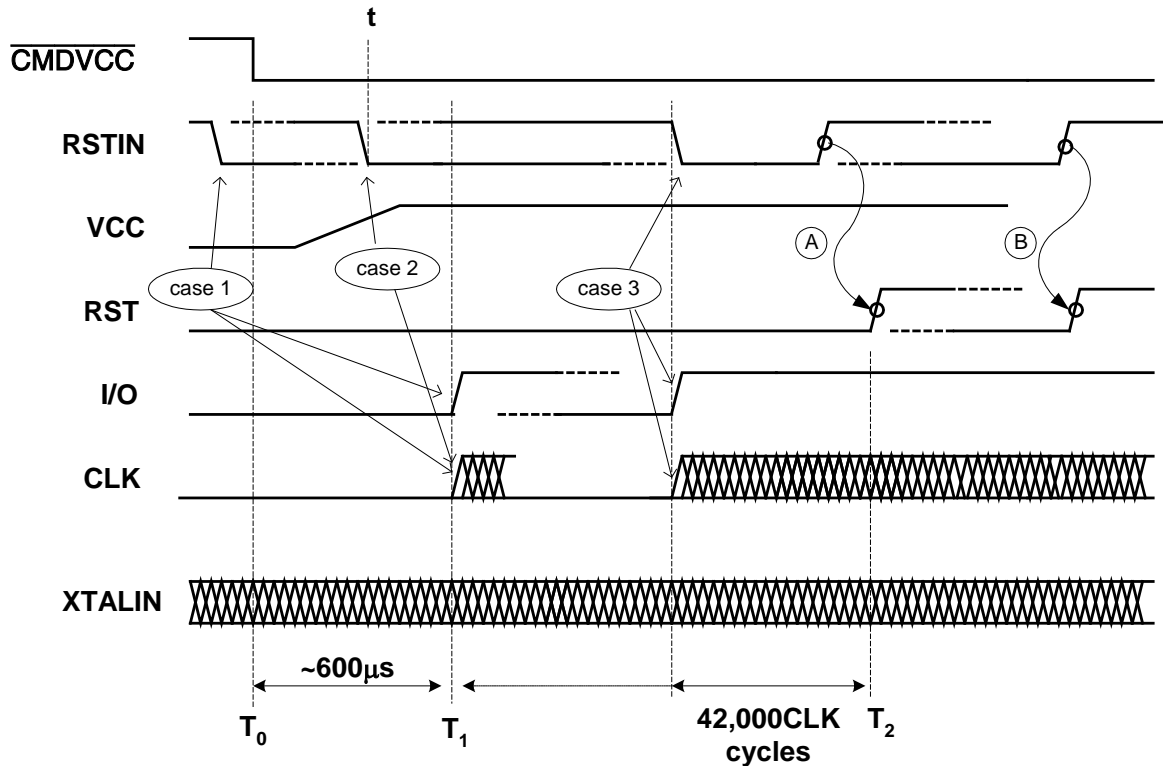


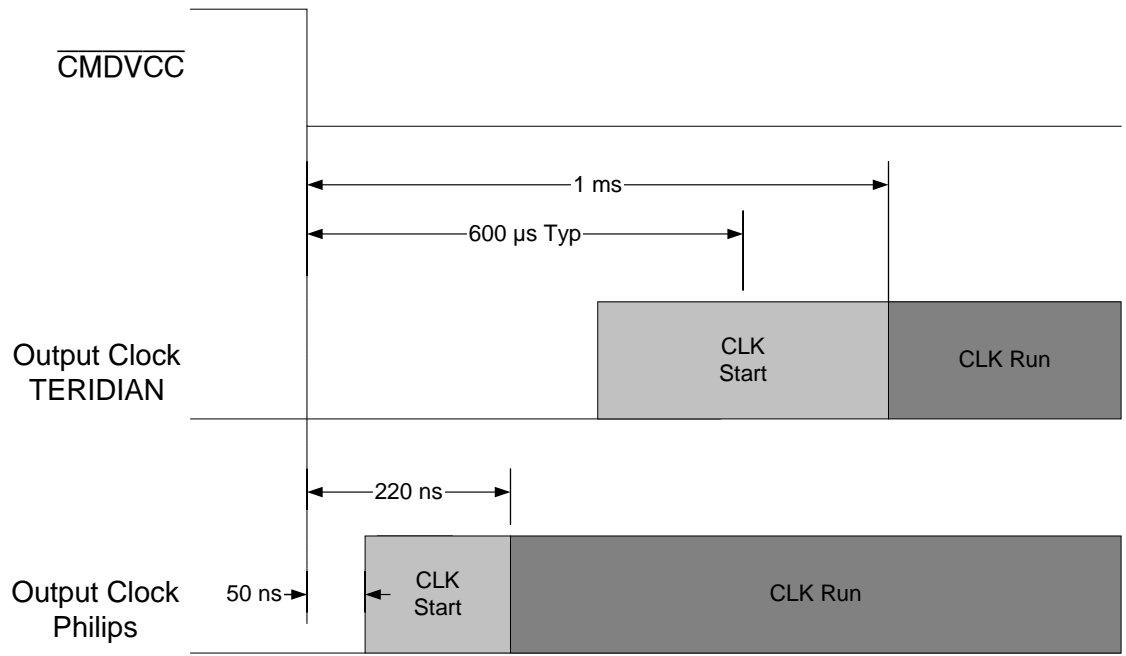
Figure 12: Teridian 73S8024RN Activation Sequence

Reset Signal Precautions

Due to activation sequence timing differences between the TDA8024T and the Teridian 8024RN, there is a possibility of an ATR timeout error occurring with the Teridian 8024RN when it replaces the TDA8024T in an application. This potential error can be eliminated by simply by extending the ATR timeout by a small amount. This extension is legal under EMV, ISO and NDS specifications. The following sections will describe these differences and the necessary modifications in detail.

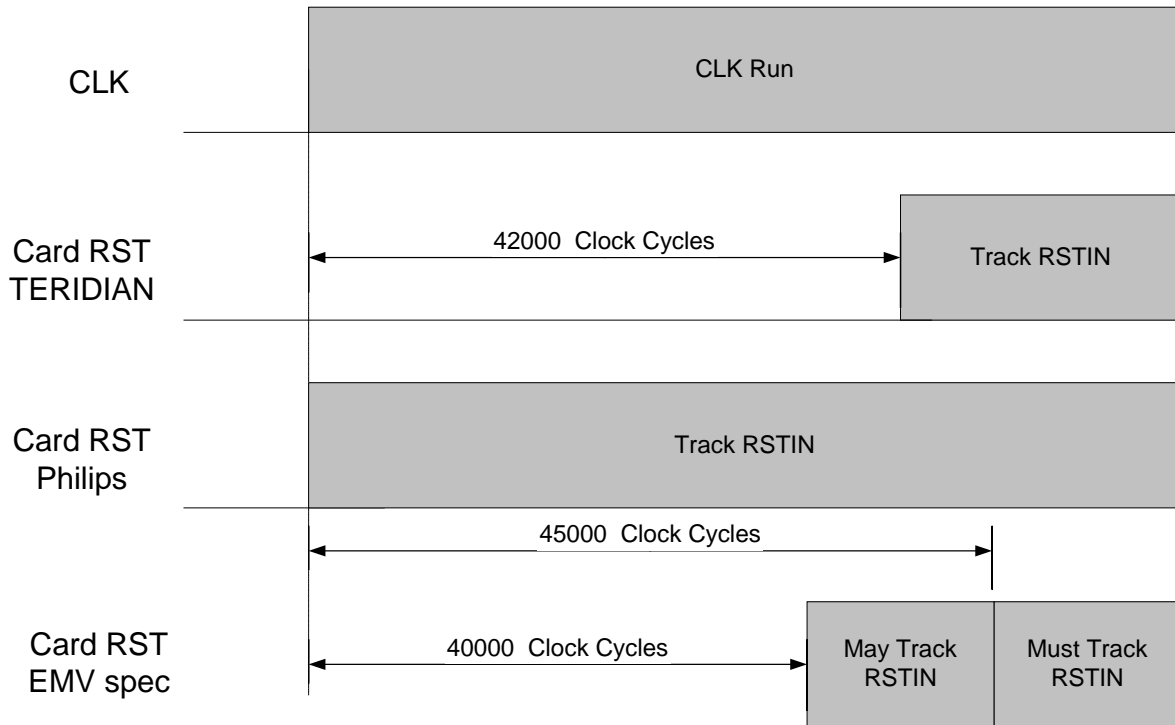
Clock Start Timing Differences

The TDA8024T will start the card CLK between 50 and 200ns after the falling edge of $\overline{\text{CMDVCC}}$, whereas the Teridian 8024RN will start the CLK around 600 μs after. The specification for the Teridian 8024RN is 1 ms maximum. As a result, the Teridian 8024RN CLK signal can start as much as 1 ms – 50 ns = **999.95 μs** (worst case maximum) after the TDA8024T.



RST Timing Differences

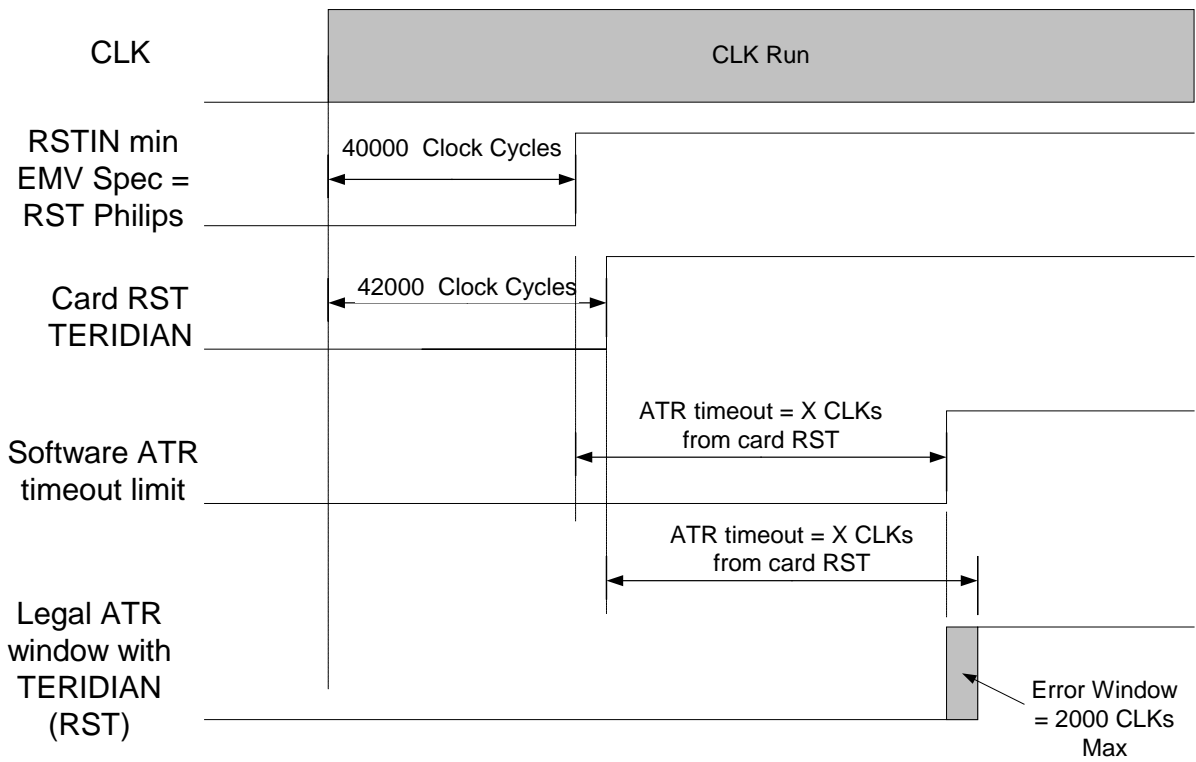
The TDA8024T doesn't have any built-in RST out delay with respect to CLK. As a result, the system controller must generate the RSTIN signal somewhere between 40000 and 45000 clock cycles after the CLK signal starts (EMV specification). The Teridian 8024RN will delay the RST signal at least 42000 clock cycles after CLK starts. If the system controller de-asserts RSTIN after 42000 clock cycles, the timing of the rising edge of RST is the same between the TDA8024T and the Teridian 8024RN.



Once card RST is de-asserted, the system controller expects an ATR response from the card within a certain window of time. If the ATR is not properly received before the end of this window an ATR timeout error will occur.



With the TDA8024T, this timeout starts at the rising edge of RSTIN. If the system controller de-asserts RSTIN between 40000 and 42000 clock cycles after CLK starts, the card RST signal timing will be different between the TDA8024T and the Teridian 8024RN.



Due to the timing difference between the devices in the case of RSTIN being de-asserted between 40000 and 42000 clock cycles after CLK, there is a delay between RSTIN and card RST up to 2000 clock cycles. This means that a card can respond with a valid ATR response (with respect to card RST) and still generate an ATR timeout error (with respect to RSTIN)

This 2000 clock cycle difference in addition to the maximum 950 us clock start timing differential need to be added to the ATR timeout to ensure the ATR timeout error will not be generated when the card responds with a valid ATR response.

Pin Comparison

Table 2 lists the 28 pins of the 73S8024RN device (SO28) and of the NXP TDA8024T device. The Comments column describes the system-level differences that should be taken into account when the 73S8024RN is used as a replacement or for dual-source designs.

Table 2: Pin Comparison

Pin No.	Interface	Pin Name		Comments
		73S8024RN	TDA8024T	
11	Smart-Card	I/O	I/O	Internal Pull-up: 11 k Ω .
13		AUX1	AUX1	
12		AUX2	AUX2	
16		RST	RST	
15		CLK	CLK	
10		PRES	PRES	All 3 ICs include static high-impedance pull-down/up resistors to allow No-Connect when unused.
9		$\overline{\text{PRES}}$	$\overline{\text{PRES}}$	
17		VCC	VCC	73S8024RN: Decouple to GND with either 1 μF (NDS or ISO-7816) or 3.3 μF (EMV) low ESR capacitor. TDA8024T: Requires 220 nF + 100 nF decoupling capacitor.
14		GND	CGND	
19	System Controller	$\overline{\text{CMDVCC}}$	$\overline{\text{CMDVCC}}$	
3		5V/ $\overline{3\text{V}}$	5V/ $\overline{3\text{V}}$	73S8024RN: Can be left open for 5 V card operation. TDA8024T: Must pulled-up for 5 V card operation.
7		CKSTOP	S1	73S8024RN: Active high control input for card clock stop. Can be left open when unused. TDA8024T / TDA8024T: Return connection for charge pump capacitor.
8		CKLVL	VUP	73S8024RN: Clock Level, to be used to in conjunction with CLKSTOP. Can be left open when unused. TDA8024T: Requires 1 x 100 nF low ESR decoupling capacitor to PGND.
1		CKDIV1	CLKDIV1	Teridian 73S8024RN has high impedance pull-down.
2		CKDIV2	CLKDIV2	Teridian 73S8024RN has high impedance pull-down.
23		$\overline{\text{OFF}}$	$\overline{\text{OFF}}$	Interrupt output Internal Pull-up: 20 k Ω .
20		RSTIN	RSTIN	
26		I/OUC	I/OUC	Internal Pull-up: 11 k Ω .
27		AUX1UC	AUX1UC	
28		AUX2UC	AUX2UC	

Table 2: Pin Comparison (continued)

Pin No.	Interface	Pin Name		Comments
		73S8024RN	TDA8024T	
24	Power Supply and Misc.	XTALIN	XTAL1	
25		XTALOUT	XTAL2	
18		V _{DDF_ADJ}	PORADJ	This pin can optionally be used in 73S8024RN and TDA8024T to modify the voltage threshold level of the internal voltage supervisor to deactivate the card interface. With both parts, this pin can be left open to retrieve the default threshold level: 73S8024RN: 2.3 V TDA8024T: 2.45 V Connecting an external resistor network to pin 18 allows modification of the V _{DD} fault threshold level. Refer to respective data sheets for determination of the resistor value (different values between 73S8024RN and TDA8024T).
5		N/C	S2	73S8024RN: No Connect TDA8024T: Requires 1 x 100 nF low ESR Charge Pump capacitor.
21		V _{DD}	V _{DD}	73S8024RN: V _{DD} = 2.7 V to 5.5 V. TDA8024T: V _{DD} = 2.7 V to 6.5 V.
6		V _{PC}	V _{DDP}	73S8024RN: V _{PC} = 4.75 V to 5.5 V. (EMV or ISO-7816), 4.85 V to 5.5 V (NDS) TDA8024T: V _{DDP} = 4.5 V to 6.5 V. Both devices require 1 x 100 nF decoupling capacitor.
4		GND	PGND	
22		GND	GND	

Revision History

Revision	Date	Description
1.0	2/14/2006	First publication.
1.1	12/4/2009	Formatted to the Teridian documentation style. Replaced all instances of "Philips" with "NXP". Assigned document number AN_8024RN_058. Miscellaneous editorial changes.