

APPLICATION NOTE 4221

# How to Optimize Avalanche Photodiode (APD) Bias Range Using a DS1841 Logarithmic Resistor

*Abstract: This article describes how three external resistors on the DS1841 logarithmic resistor are used to adjust the output range of an APD bias circuit. A spreadsheet is supplied that makes the adjustment process easy.*

## APD Bias Circuit

The [DS1841](#) temperature-controlled, NV, I<sup>2</sup>C, logarithmic resistor contains one 7-bit logarithmic variable resistor. Used in conjunction with a step-up DC-DC converter, the DS1841 adjusts the bias voltage applied to an avalanche photodiode (APD). Three external resistors ( $R_{SER}$ ,  $R_{TOP}$ , and  $R_{PAR}$ ) are used to adjust the output range (**Figure 1**).

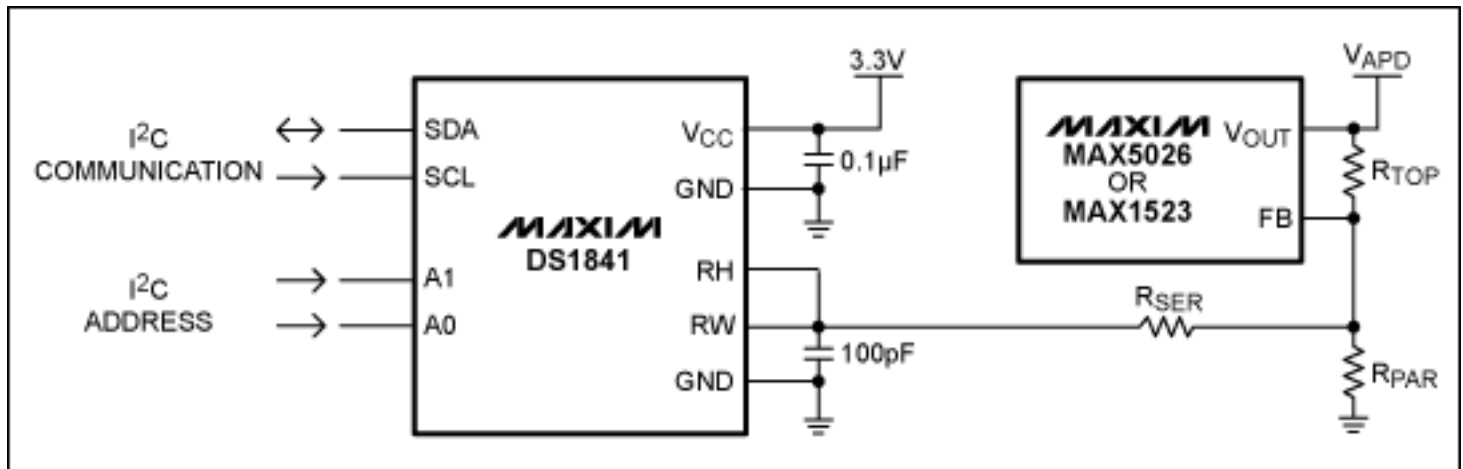


Figure 1. APD bias circuit using the DS1841 and a step-up DC-DC, here the MAX5026 or MAX1523.

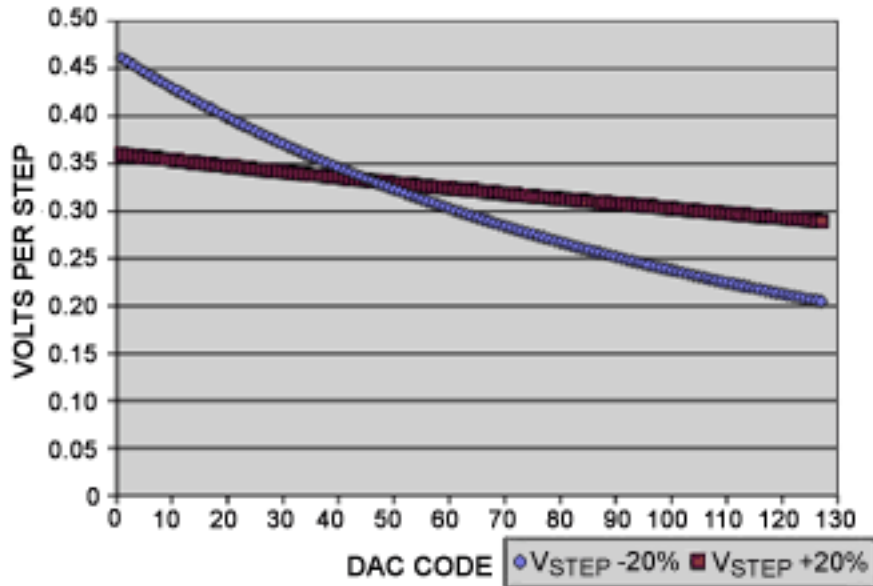
## Adjusting the APD Bias Range

A spreadsheet, [DS1841 APD Bias Range Adjustment](#) (xls), makes it easy to adjust the APD bias range. The spreadsheet has four input variables:  $R_{TOP}$ ,  $R_{SER}$ ,  $R_{PAR}$ , and  $V_{FB}$ . After inputting these resistor values, the spreadsheet then calculates four outputs:  $V_{APD}$  (max),  $V_{APD}$  (min), STEP (max), STEP (avg). It also generates two graphs: APD Bias vs. DAC Code, Volts Per Step vs. DAC Code. The interface in Figure 2 shows the four variables and the graphics generated from the values input there. **Table 1** defines the terms used in the spreadsheet.

R<sub>TOP</sub> 221kΩ  
R<sub>SER</sub> 4.99kΩ  
R<sub>PAR</sub> 10kΩ  
V<sub>REF</sub> 1.23V

V<sub>APD</sub> (max) 78.0V  
V<sub>APD</sub> (min) 40.4V  
STEP (max) 0.46V  
STEP (avg) 0.32V

### VOLTS PER STEP vs. DAC CODE



### APD BIAS VOLTAGE vs. DAC CODE

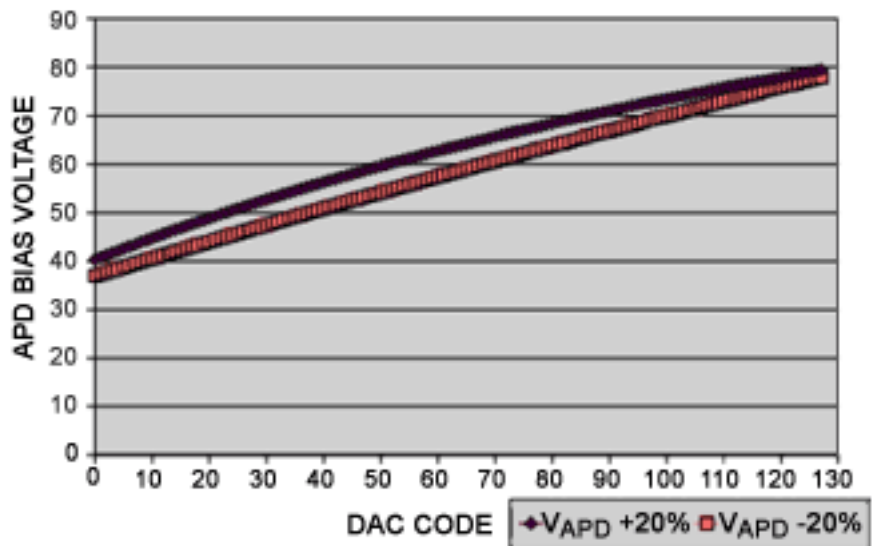


Figure 2. The spreadsheet interface with the four variables for data input, which appear at the top left.

**Table 1. Variable Definitions for APD Bias Range Adjustment with the DS1841**

$V_{FB}$	The voltage present at the feedback node of the DC-DC converter.
$V_{APD} (max)$	The maximum voltage to which the APD bias can be set under worst-case conditions.
$V_{APD} (min)$	The minimum voltage to which the APD bias can be set under worst-case conditions.
STEP (max)	The maximum calculated voltage step that can occur between two adjacent DAC codes.
STEP (avg)	The average voltage step size that occurs across the full range.
$V_{STEP} +20\%$	The voltage step size when the variable resistor is at the maximum of the process range (+20%).
$V_{STEP} -20\%$	The voltage step size when the variable resistor is at the minimum of the process range (-20%).
$V_{APD} +20\%$	The APD bias voltage when the variable resistor is at the maximum of the process range (+20%).
$V_{APD} -20\%$	The APD bias voltage when the variable resistor is at the minimum of the process range (-20%).

---

Application Note 4221: [www.maxim-ic.com/an4221](http://www.maxim-ic.com/an4221)

### More Information

For technical support: [www.maxim-ic.com/support](http://www.maxim-ic.com/support)

For samples: [www.maxim-ic.com/samples](http://www.maxim-ic.com/samples)

Other questions and comments: [www.maxim-ic.com/contact](http://www.maxim-ic.com/contact)

---

### Automatic Updates

Would you like to be automatically notified when new application notes are published in your areas of interest?

[Sign up for EE-Mail™.](#)

---

### Related Parts

DS1841: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX1523: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

MAX5026: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

AN4221, AN 4221, APP4221, Appnote4221, Appnote 4221

Copyright © by Maxim Integrated Products

Additional legal notices: [www.maxim-ic.com/legal](http://www.maxim-ic.com/legal)