

APPLICATION NOTE 4040
User's Guide to the DS28DG02

Abstract: The DS28DG02 is a 2kb SPI™ EEPROM with PIO, real-time clock (RTC), reset, battery monitor and watchdog that combines several functions needed in portable equipment and embedded applications. This application note supplements the product's data sheet, gives additional information on the SPI interface and its write-protection scheme, and shows how to use the device's 12 PIOs and the RTC alarm function. The document also includes guidance on battery selection, shielding of the RTC crystal pads, and the software response to alarm events.

Communication Interface

The [DS28DG02](#) is a slave EEPROM device which gives the master, typically a microcontroller, access to its resources through a serial peripheral interface (SPI). SPI was originally created by Motorola for the MC68HCxx line of microcontrollers. **Table 1** shows the standard SPI signal names and their function.

Table 1. SPI Signal Names

Motorola Name	Function	Alternate Names
SCLK	Serial clock, push/pull driver, generated by the master. An open-drain driver is permissible if the rise-time and fall-time specifications are met.	SCK, SK, C
MISO	Data line slave to master, "master-in slave-out." A push/pull output with high-impedance, driven by the slave, is connected to the master's serial input.	SO, DO, Q
MOSI	Data line master to slave, "master-out slave-in." A push/pull output, driven by master, is connected to the slave's serial input.	SI, DI, D
Active-low SS	Slave select, push/pull output, generated by the master.	CSZ, active-low CS

The basic SPI communication concept employs shift registers at both master and slave. The inputs and outputs of the shift registers are wired to form a circle, as shown in **Figure 1**. A clock signal, driven by the master, shifts serial data in blocks of eight bits simultaneously from master to slave and from slave to master, thereby making SPI a full-duplex protocol. Most SPI slaves, however, including the DS28DG02, first require a command before they can receive or send data. As a consequence, data is transported either from master to slave or from slave to master in a half-duplex fashion.

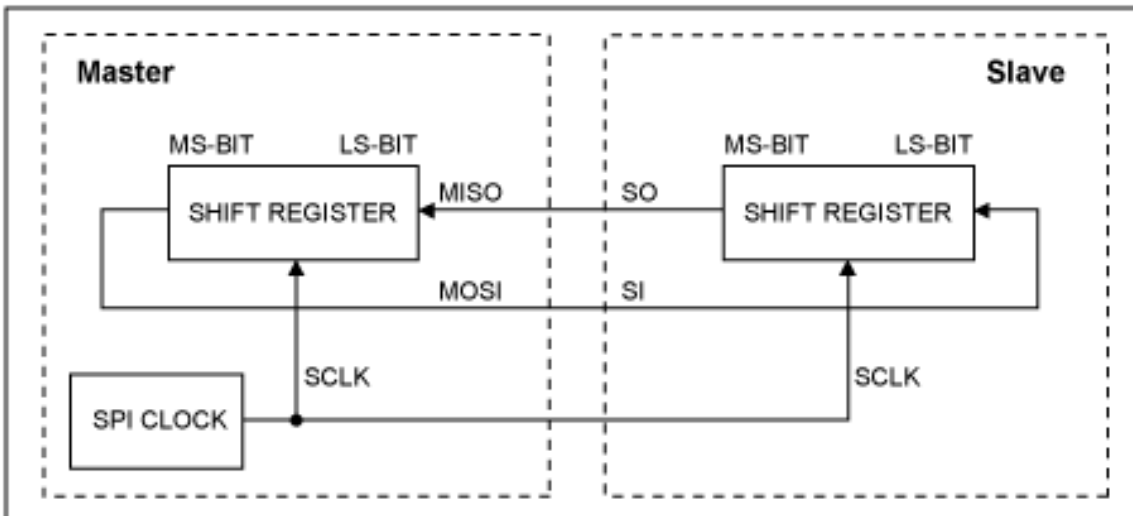


Figure 1. SPI communication concept.

The SPI specification defines four modes, which are selected by the control bits CPOL and CPHA in the SPI master.

There is no standard on how to reference these modes. **Table 2** lists the mode definitions commonly used in SPI documentation.

Table 2. SPI Mode Definitions

SPI Mode	CPOL	CPHA	Description
0 or (0,0)	0	0	The clock idle state is low. Data is captured on the rising clock edge and shifted out on the falling clock edge.
1 or (0,1)	0	1	The clock idle state is low. Data is captured on the falling clock edge and shifted out on the rising clock edge.
2 or (1,0)	1	0	The clock idle state is high. Data is captured on the falling clock edge and shifted out on the rising clock edge.
3 or (1,1)	1	1	The clock idle state is high. Data is captured on the rising clock edge and shifted out on the falling clock edge.

The DS28DG02 supports SPI modes (0,0) and (1,1). In these modes data is captured (clocked in) on the rising clock edge and shifted out (possibly changed) on the falling clock edge. The clock state at the falling edge of CSZ tells the DS28DG02 which SPI mode the master uses. If communication is attempted in modes (1,0) or (0,1), the device's behavior is undefined.

For additional information on the SPI protocol and timing see the *SPI Interface* section in the DS28DG02 data sheet, or search the phrase "SPI slave timing" on the Internet. Documents found by this web search will mostly be about microcontrollers that can function as an SPI master or slave, depending on internal register settings. Third-party documents that give a good overview on the SPI concept and explain the setup of an SPI master are:

<http://www.mct.net/faq/spi.html> (general information)

http://www.atmel.com/dyn/resources/prod_documents/doc2585.pdf (master setup)

Write-Protection Scheme

SPI Memory devices utilize a 3-level scheme to protect the memory from inadvertent or unauthorized changes: the WEN bit in the SPI Status register; the Block write-protection using control bits in the SPI Status register; and the hardware write-protection using a pin state and an enable bit in the SPI Status register. The Register write-protection, unique to the DS28DG02, is on the same level as the Block write-protection, but applies to a different memory area. **Table 3** shows the control bits and their effect on memory.

Table 3. Write-Protection Control

Level	Controlling Bits	Memory Protected
1	WEN	All writeable memory addresses and the SPI Status register
2	BP1:BPO	Addresses 000h to 0FFh
2	RPROT	Addresses 120h to 135h
3	WPEN (in conjunction with WPZ pin state)	SPI Status register, nonvolatile bits only

Level 1: WEN Bit in the SPI Status Register

This bit is cleared on power-up, after a successful completion of any write-function command, or through the SPI command WRDI (write disable). The only way to set the WEN bit is through the SPI command WREN (write enable).

Note: The WEN bit concept prevents corruption of writeable memory in case the SPI master malfunctions.

Level 2: BP1:BPO Bits in the SPI Status Register

This common method of write-protection uses two nonvolatile bits of the SPI Status register (BP1:BPO) to write-protect none, all, the upper half, or the upper quarter of the EEPROM. Since the controlling bits are located in the SPI Status register, they are subject to the Hardware write-protection. Without Hardware write-protection, the Block write-protection can be changed through software control. **Note:** The Block write-protection configures some EEPROM as read-only, while leaving the remaining EEPROM available for the master to store data that can change during normal operation of the end product.

Level 2: RPROT Bit in the SPI Status Register

A special function of the DS28DG02, this method uses the nonvolatile RPROT bit of the SPI Status register to write-protect the user-writeable bytes in the address range from 120h and higher. If RPROT is 1, these addresses are write-protected. This protects the RTC, the RTC Alarm registers, the Multifunction Control/Setup register, and the Alarm/

Status register and prevents writing to the PIOs. This level of write-protection does not protect the power-on default values of the PIO-related registers, which are stored from 10Ah to 10Fh. Since the RPROT bit is located in the SPI Status register, it is subject to the Hardware write-protection. Without Hardware write-protection, RPROT can be changed through software control. **Note:** Register write-protection prevents accidental changes to the RTC and its alarms, and to the register that defines the functionality of the DS28DG02 in the end product (e.g., watchdog, battery monitor, RTC).

Level 3: WPEN Bit in the SPI Status Register

This method uses the WPZ pin in conjunction with the WPEN bit in the SPI Status register. This function protects only the nonvolatile bits of the SPI Status register, in particular the block protection bits BP1:BP0, RPROT, and WPEN. The WPEN bit, if set to 1, enables the WPZ pin to control the protection of all nonvolatile bits in the SPI Status register, including WPEN. With a factory-fresh SPI memory device the WPEN bit reads 0. This allows programming the memory on a board tester even if the WPZ pin tied to ground. In the last step, after the memory is programmed, the tester then sets the level 2 protection and writes the WPEN bit to 1, thereby activating the hardware write-protection. As long as the logic state at the WPZ pin remains at 0, the nonvolatile bits of the SPI Status register remain write-protected. To change any of the nonvolatile bits, the logic state at the WPZ pin must be changed to 1, e.g., through a jumper that temporarily connects the pin to V_{CC}. **Note:** Hardware write-protection makes the level 2 protection settings permanent but still leaves a backdoor (the WPZ pin) for later corrections.

Note: With Register write-protection permanently enabled, the only way to clear the watchdog, RTC, and battery alarms is through V_{CC} power cycling. Replacing the battery, regardless of V_{CC} power, clears the Multifunction Control/Setup register and the RTC with its alarm registers. If both Hardware write-protection and Register write-protection are activated (RPROT = 1, WPEN = 1, WPZ pin at GND), the user may need to make a service call to the equipment manufacturer to get the equipment reconfigured and running.

Battery Selection

The DS28DG02 needs a battery to maintain its configuration stored in the Multifunction Control/Setup register at address 134h, and to keep its RTC running. If V_{CC} is permanently available, no battery is needed and the V_{BAT} pin is tied to V_{CC}. If V_{CC} is interrupted and there is no battery backup, the Multifunction Control/Setup register powers up with all bits at 0. That action halts the RTC and disables the clock alarm, watchdog, and battery monitor. This is the normal setup and no reason for concern in applications that do not use the RTC and watchdog. Typical DS28DG02 applications use at least the RTC or the watchdog, thus requiring a battery that should be monitored.

Battery power is consumed only if V_{CC} is switched off. There are two situations to note: a) when the RTC oscillator is halted (off, OSCE = 0); and b) when the RTC oscillator is on (running, OSCE = 1). There is, theoretically, also a third case concerning the battery monitor. However, the peak load on the battery from the battery monitor (I_{MAX} = 20μA) applies only for 2s each hour, resulting in an average load current of 11nA (20μA × 2/3600), which is more than two magnitudes lower than the load with the RTC switched off. The battery monitor does not reduce the battery lifetime because the monitoring takes place only while V_{CC} is applied, and the RTC and other nonvolatile memory cells are powered from V_{CC}, not from the battery.

The typical battery voltage for the DS28DG02 is 3V, supplied by a single lithium cell (Li+) or two silver oxide coin cells in series. The energy capacity of these batteries is commonly specified in mAh (milliampere-hours). The value is obtained by using a load resistor, similar to that in the intended application, to measure the time it takes for the battery voltage to fall below a defined threshold. Details are found in data sheets from battery manufacturers:

<http://www.panasonic.com/industrial/battery/oem/chem/lith/coin1.htm>

http://www.rayovac.com/technical/pdfs/pg_lithium.pdf

<http://data.energizer.com/DataSheets.aspx>

Assuming that a battery is similar to a capacitor, the duration to discharge a battery is calculated as $t = Q/I$. If, for example, the battery holds 1mAh and the discharge current is 1μA, the discharge time is:

$$\frac{1 \times 10^{-3}\text{Ah}}{1 \times 10^{-6}\text{A}} = 1000\text{h} = 1000/24\text{days} = 41.66\text{days} \quad (\text{Eq. 1})$$

This result can be scaled for battery capacity and discharge current using the following equation:

$$\text{Lifetime} = \frac{\text{Capacity (in mAh)}}{\text{Current (in } \mu\text{A)}} \times 41.66 \text{days} \quad (\text{Eq. 2})$$

If the load current is 10 μ A, for example, a 48mAh battery keeps the RTC running for 48/10 \times 41.66 or 200 days. Around +25°C the load current with RTC on is 4.7 μ A maximum. The same battery would, therefore, last for:

$$48/4.7 \times 41.66 = 425 \text{days or } 1.17 \text{years} \quad (\text{Eq. 3})$$

Using two battery cells in series doubles the available voltage and energy, but not the battery's lifetime. To determine the lifetime, the capacity of the single cell must be inserted into Equation 2 since the current flows through each of the cells in series, discharging each at the same rate.

Using the PIOs

The DS28DG02 has 12 PIO channels. In a typical application, some PIOs are used as input, others as output, and some are not used at all. PIOs that are "neighbors" in the memory map (PIO0 to PIO7, PIO8 to PIO11) are not neighbors on the circuit board. With the TSSOP, all even-numbered PIOs are on the left side and the odd-numbered PIOs on the right side of the package. With the TQFN there are three even-numbered PIOs on the west side, three odd-numbered PIOs on the east side, and the remaining six PIOs, even and odd, at the south side of the package. Although this can appear unusual at the first glance, it does not affect the usability of the device.

If none of the PIOs in output mode needs to sink or source high currents, the low-current output mode is applicable. The low-current output mode is where PIO reading and writing occurs simultaneously for all PIOs that share the same memory address. If five to eight PIOs need to be read or written simultaneously, select PIO channels 0 to 7 and assign them to the nodes in the application according to what best fits the topology of the board layout. Since writing in high-current mode is not simultaneous, assign the PIOs only for optimal board layout. The following example shows one approach to assigning PIO channels.

Example Configuration

Outputs: 6
 Output type: 4 push/pull, 2 open-drain
 Output mode: Low current (simultaneous writing)
 Inputs: 4
 Read inversion: None
 Not used: 2 PIOs

Viewing the DS28DG02's PIO pin assignment in a counter-clockwise manner, the sequence of PIOs sharing the same memory address is 0, 4, 6, 2, 3, 7, 5, 1. This sequence is independent of the package type. Obvious close neighbors are channels 6, 2, 3 and 7. For the remaining two outputs, we assign channels 0 and 4, because they are adjacent pins. This approach leaves channels 1 and 5 unused. The output type is set for groups of four PIOs, 0 to 3, 4 to 7 and 8 to 11; PIOs within a group have the same output type. Four outputs in the example need to be push/pull. With the assignments just made, these could be channels 0 to 3 or 4 to 7. Since channel 1 is not used and leaves only channels 0, 2 and 3, this output type requirement cannot be met.

To meet the output type requirements, the channel assignment must therefore be changed. Channels 4 to 7 are now used for push/pull (arbitrary choice) and channels 2 and 3 for open-drain. This leaves channels 0 and 1 unused. The inputs are assigned to channels 8 to 11, which also share a memory address.

Next, the power-on default register values must be defined for this configuration and written to the respective memory addresses. The tables below use the following color codes to explain the choice.

	Value resulting from configuration/application requirements
	Arbitrary assignment, "don't care" condition
	(Not assigned, reserved)

Power-On Default for PIO Output State

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
10Ah	0	0	1	1	1	1	0	0	3C
10Bh	0	0	0	0	0	0	0	0	00

Note: For this example, the assumption is made that the application requires channels 2 to 5 to power up with logic 1 and channels 6 and 7 with logic 0.

Power-On Default for PIO Direction

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
10Ch	0	0	0	0	0	0	1	1	03
10Dh	0	0	0	0	1	1	1	1	0F

Power-On Default for PIO Read Inversion (PIO0 to PIO7)

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
10Eh	0	0	0	0	0	0	0	0	00

Power-On Default for PIO Read Inversion (PIO8 to PIO11), PIO Output Type, and Output Mode

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
10Fh	0	0	0	1	0	0	0	0	10

Using the definitions for the communication examples in the data sheet, the following sequence updates to the PIOs that are defined as outputs:

SEL	WREN	DSEL	SEL	WRITEH	<20h>	<1 byte PIO data>	DSEL
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To generate a waveform pattern at the PIOs it is not necessary to repeat the full sequence with different PIO data. Instead, send as many PIO data bytes as desired; the first, third, fifth, etc., byte is used to update the PIOs. The other bytes (second, fourth, sixth, etc.) have no effect since PIOs 8 to 11 are assigned as inputs.

The following sequence reads from the PIOs that are defined as inputs:

SEL	READH	<27h>	<1 bytes PIO data>	DSEL
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To read from the PIOs repeatedly at a fast rate, it is not necessary to repeat the full sequence. Instead, use the starting address 126h and read as many bytes as desired. The first, third, fifth, etc., byte returns the state of the channels defined as output. The other bytes (second, fourth, sixth, etc.) report data from PIOs 8 to 11, which are assigned as inputs.

PIO High-Current Mode

For write access, the PIOs can operate in low-current mode or in high-current mode. The mode selection applies to all PIO lines in the same manner. In low-current mode all PIOs sharing the same byte address switch simultaneously. In addition, if the PIOs are accessed starting with a write to address 120h, the write address toggles between 120h (PIO0 to PIO7) and 121h (PIO8 to PIO11) for every data byte that the DS28DG02 receives. This approach allows fast writing to the PIOs, thus eliminating the mandatory WREN command before the next write access.

The current sink or source capability of the PIOs is the same in both high- and low-current modes. However, in high-current mode (OTM = 1), the PIOs switch sequentially, one channel at a time; the slew rate of the PIO current is limited by active circuitry. Address toggling does not apply in high-current mode. Instead, the address just increments from 120h to 121h, and then to 122h, and so on. To write to address 120h again, a new write sequence is necessary.

If the DS28DG02 has a stable V_{CC} supply and generates a reset immediately after switching PIOs, inductive voltage spikes get into the V_{CC} monitor and are mistaken for a power failure. In this case either high-current mode must be used, or the software must simulate high-current mode by switching less than eight channels at a time, thereby ensuring that the change in current flow does not exceed the maximum rating of $\pm 50\text{mA}$.

RTC Crystal and PCB Layout

32KHz watch crystals are offered in various package types and sizes. The PCB layouts shown in the DS28DG02 data sheet assume that the spacing of the crystal leads matches that lead pitch (TSSOP—0.65mm; TQFN—0.50mm). This is a very tight spacing, and such small crystals may not be easily available. To accommodate larger crystals the PCB layout needs to be modified as indicated in **Figure 2**. It is important to maintain the guard ring and the local ground plane. The traces from the crystal pins X1 and X2 to the crystal pads should be kept symmetric.

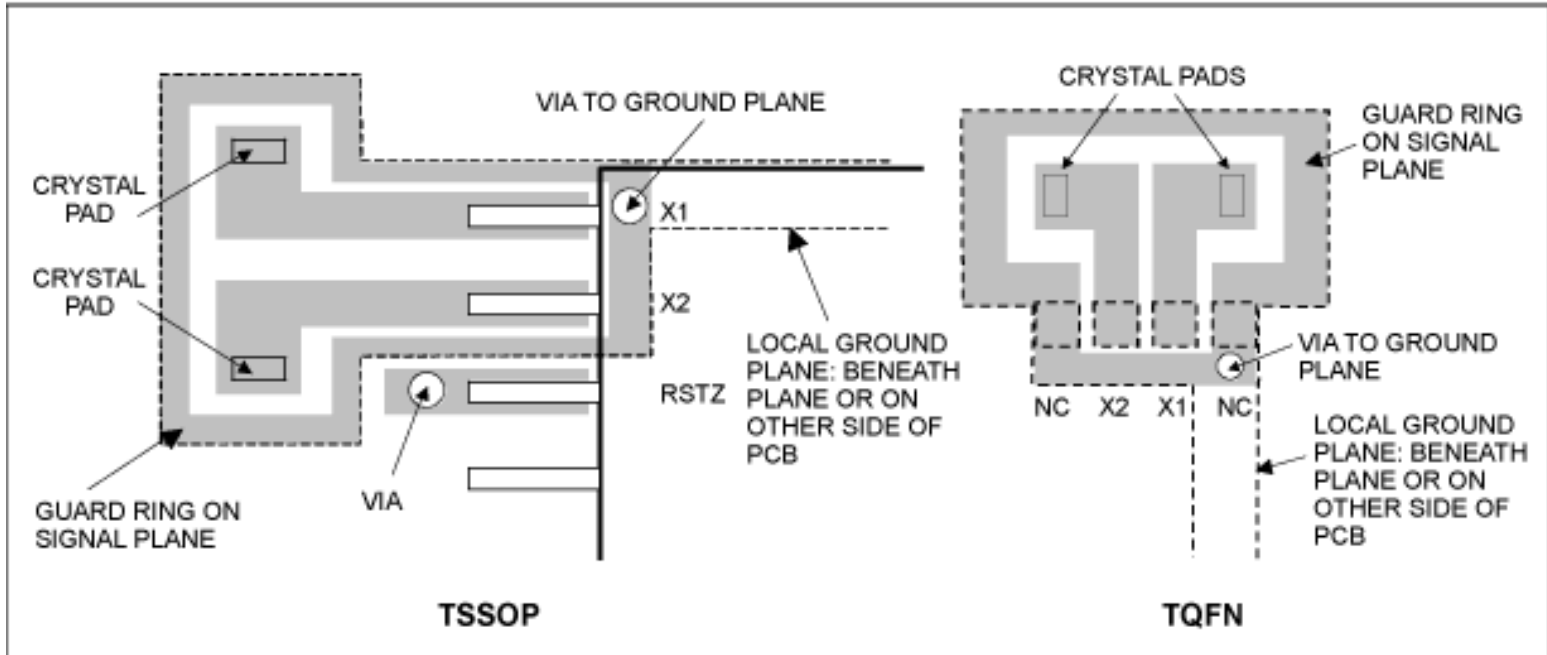


Figure 2. Alternative PCB layout.

For additional information on crystal selection, see Maxim's Application Note #616, [Considerations for Maxim Real-Time Clock Crystal Selection](#). This document also includes technical data on SMD crystals and links to several vendor websites.

Clock Alarms

The DS28DG02 can generate RTC alarms from once a second to once a month. The alarm is signaled through the ALMZ pin, which is shared with the battery alarm and the watchdog alarm. As a precondition for clock alarms, the RTC must be running and clock alarms enabled ($OSCE = 1$, $CAE = 1$).

Generally, for a clock alarm to go off, the clock's state must match the value in the alarm registers. There are four RTC Alarm registers: seconds, minutes, hours, and day of week or day of month. The most significant bit of the Alarm registers, referenced AM1 to AM4, controls whether the register participates in the comparison. The DY/DT bit at address 133h specifies whether the remaining six bits are to be compared to the RTC's day of the week or day of the month. In all other aspects the alarm registers match the bit assignments of the RTC.

After the time and frequency of the alarm are defined, the data for the clock Alarm registers is easily created by writing the individual bits (BCD code) into the template and converting the result into hexadecimal format (column "Hex"). The resulting data is then written to the Alarm registers through a SPI write sequence. The examples below illustrate the process. The color codes here represent the same assignments as in the PIO section above.

Example 1: Alarm Every Hour at 25 Minutes 30 Seconds

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
130h	0	0	1	1	0	0	0	0	30
131h	0	0	1	0	0	1	0	1	25
132h	1	0	0	0	0	0	0	0	80
133h	0	0	0	0	0	0	0	0	00

Note: For alarms every hour, minute, or second, the 12/24 bit (bit 6 at address 132h and 12Bh) does not apply. To generate an alarm every minute at 30 seconds, change bit 7 at address 131h to 1. This excludes the minutes from the comparison.

Example 2: 24-Hour Format, Alarm Every Day at 22:59:59

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
130h	0	1	0	1	1	0	0	1	59
131h	0	1	0	1	1	0	0	1	59
132h	0	0	1	0	0	0	1	0	22
133h	1	0	0	0	0	0	0	0	80

Example 3: 12-Hour Format, Alarm on the First Day of the Week at 6:30:00PM

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Hex
130h	0	0	0	0	0	0	0	0	00
131h	0	0	1	1	0	0	0	0	30
132h	0	1	1	0	0	1	1	0	66
133h	0	1	0	0	0	0	0	1	41

Note: The day of week counter uses the codes 1 to 7. The assignment of counter value to the day of week is arbitrary. Typically, the number 1 is assigned to a Sunday (U.S.A. standard) or to a Monday (European standard).

Watchdog

A watchdog is commonly found with CPU supervisory circuits. Technically, a watchdog can be described as a retriggerable one-shot. The microcontroller needs to keep the one-shot in the unstable state by regularly applying a positive pulse at the watchdog's trigger input, WDI. If the microcontroller cannot do this, the watchdog times out and resets the microcontroller.

The DS28DG02's watchdog time-out is selected through the WD1:WD0 bits of the SPI Status register. The watchdog is activated by writing the WDE bit at address 134h to 1, provided that write access to the registers is not blocked (RPROT = 0). Whenever a watchdog goes off, the WDA bit in the Alarm and Status register at address 135 is set; the WDOZ pin (default) or the ALMZ pin (alternate choice), which is shared with the clock alarm and the battery monitor, and the RSTZ pin go low.

Attaching a battery (battery attach) or power-on reset (if there is no battery) disables the watchdog (WDE = 0). Once activated by writing the WDE bit to 1, the watchdog remains enabled through battery backup even if V_{CC} is switched off. When V_{CC} ramps up or after setting the WDE bit, the watchdog's internal counter is cleared, thus giving the microcontroller time to complete its power-up routine before the watchdog needs to be retriggered.

Response to Alarms

The DS28DG02's Alarm and Status register at address 135h holds six bits that indicate important events. Upon such an event, the microcontroller should respond with a specific action, as listed below. All alarms are cleared by writing to this register, provided that RPROT = 0.

RST: Reset Flag	This bit is set whenever there is a pulse at the RSTZ pin, e.g., power-on reset when V_{CC} ramps up, at manual reset, or at watchdog alarm. The microcontroller responds by executing its normal power-on routine.
WDA: Watchdog Alarm	Since the watchdog alarm resets the microcontroller, the same response as for RST applies. The microcontroller could count the number of watchdog alarm events.
CLKA: Clock Alarm	Upon a clock alarm, the microcontroller responds with an application-specific action.
BOR: Battery-On Reset Flag	When the battery is attached, the Multifunction Control/Setup register, the RTC, and the RTC Alarm registers are cleared. This is an error condition that requires the execution of an initialization procedure to restore the lost values, e. g., through user input (time) and backup values stored in EEPROM. If Hardware write-protection is active and RPROT = 1, the equipment may have to be returned for service unless the user knows how to disable the Hardware write-protection. The microcontroller can monitor the Hardware write-protection through the WPZV bit.
POR: Power-On Reset Flag	Power-on reset generates a pulse at the RSTZ pin. The microcontroller responds by executing its normal power-on routine.
BATA: Battery Alarm	This alarm indicates that the backup battery is near the end of its lifetime. This condition requires that the user be alerted to replace the battery. Depending on the application, one could count the battery alarm events and, after a certain count, stop the equipment from operating until the battery is replaced.

Conclusion

The DS28DG02 is a very flexible and easy-to-use component for portable equipment and other applications that require memory, RTC, PIOs, and CPU supervisory functions such as power monitor and watchdog.

SPI is a trademark of Motorola, Inc.

Application Note 4040: <http://www.maxim-ic.com/an4040>

More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

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Related Parts

DS28DG02: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

AN4040, AN 4040, APP4040, Appnote4040, Appnote 4040

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