



APPLICATION NOTE 3997

How to Achieve a 300:1 Dimming Ratio with the DS3881/DS3882 CCFL Controllers

Abstract: This application note describes how CCFL lamps can be dimmed and how a user can maximize the dimming ratio of a CCFL inverter by using the DS3881 and DS3882 CCFL controllers. The note offers guidelines for practical implementations in automotive, industrial, and avionics applications.

Introduction

The DS3881 and DS3882 are controllers for cold-cathode fluorescent lamps (CCFLs) that backlight liquid crystal displays (LCDs) in automotive, industrial, and avionics applications. These design systems often require a wide dimming ratio. An example is in automotive applications where the LCD panel must be easily readable in bright sunshine and dark tunnels. The DS3881 and DS3882 allow the user to create a CCFL inverter with a dimming ratio of 300:1 or greater.

Dimming CCFL Lamps

CCFLs can be dimmed using either amplitude modulation or pulse-width modulation (PWM). In this application note, amplitude modulation is referred to as analog dimming, and pulse-width modulation is referred to as digital dimming.

Analog dimming reduces the amount of current flowing through the lamps. While useful, this technique has a very limited dimming range. If the current in CCFL lamps is reduced by more than about one-third of their rated nominal lamp current, the lamps start to exhibit some undesirable characteristics. Specifically, the lamp current waveforms become unbalanced and irregular. If a CCFL lamp is rated for 6mA_{RMS} , for example, reducing the lamp current below about 2mA_{RMS} can result in poor lamp performance. Thus, this basic lamp characteristic prevents the analog dimming technique from achieving a dimming ratio of greater than about 3:1.

Digital burst PWM dimming turns the lamps on and off at a rate faster than the human eye can detect. If the lamps are turned on for a very short period of time (i.e., a burst), a dimming ratio of 100:1 or greater can be achieved. Together, the CCFL lamp frequency, the digital burst PWM dimming frequency, and the minimum number of lamp-on burst cycles determine the maximum digital dimming ratio possible. CCFL lamps have a relatively slow response time of about $50\mu\text{s}$ to $75\mu\text{s}$, which limits the minimum burst on-time. If the burst on-time is reduced to less than the lamp response time, then active control of the lamp is compromised.

Neither the analog nor the digital dimming technique alone can achieve a 300:1 dimming ratio.

Dimming CCFL Lamps Using the DS3881 and DS3882

The DS3881 and DS3882 CCFL controllers use both analog and digital dimming techniques to obtain a 300:1 or greater dimming ratio. To achieve this large dimming ratio, users must operate the devices in the software-control mode using the I²C interface because the analog dimming functionality can only be accessed through the I²C bus.

In the DS3881 and DS3882, the digital dimming can be controlled by either the internal BPWM register or an external PWM applied at the PSYNC input. The analog dimming is controlled by the internal BLC register. Please

see the [DS3881](#) and [DS3882](#) data sheets for more details on how to select and control each mode.

The DS3881 and DS3882 have two unique features that allow the user to reduce the minimum number of lamp cycles during a burst dimming cycle. First, the number of soft-start lamp cycles can be set at the beginning of each burst dimming cycle from 0 to 16 lamp cycles in increments of 2 lamp cycles. This feature is controlled by the internal SSP1 to SSP4 registers. To minimize the number of lamp cycles in each burst dimming cycle, the user can completely remove the soft-start cycles by setting the MDC codes in SSP1 to SSP4 to 0h. This action will set the soft-start profile to 0 lamp cycles. Alternatively, the number of soft-start lamp cycles can be set to 2, 4, 6, 8, 10, 12, 14, or 16, as needed.

The user can also select the rate at which the device samples the lamp current. This is accomplished using the LSR0 and LSR1 control bits in Control Register 2 (CR2). The lamp sample rate can be set to either 4, 8, 16 or 32 lamp frequency cycles. To minimize the number of lamp cycles in each burst dimming cycle, the user can set the lamp sample rate to 4 lamp frequency cycles.

The formula below can be used to estimate the maximum dimming ratio possible when using just PWM digital burst dimming.

$$(\text{Lamp Frequency}/\text{Dimming Frequency})/(\# \text{ of Soft-Start Lamp Cycles} + \text{Lamp-Cycle Sample Rate}) \quad (\text{Eq. 1})$$

The lamp frequency is usually determined by system criteria which can include LCD video interference issues, EMI issues, or efficiency. Consequently, it is not easy to change the lamp frequency to optimize the system dimming ratio. To maximize the dimming ratio, the dimming frequency should be minimized. But there is a caveat to this: reducing the dimming frequency below about 100Hz can cause flicker because the human eye begins to detect the lamps turning on and off.

As an example, consider a system with a lamp frequency of 60kHz and a burst dimming frequency of 100Hz. **Figures 1** through **3** detail the lamp current at minimum burst dimming. In this example, the soft-start was set to 2 lamp cycles (SSP1 = 00h, SSP2 = 00h, SSP3 = 00h, SSP4 = 70h), and the lamp-sample cycle rate was set to 4 lamp cycles (LSR0 = 0/LSR1 = 0). If the soft-start was reduced to 0 lamp cycles, the resulting minimum burst would only be 4 lamp cycles. At a lamp frequency of 60kHz, this would only provide the lamp a response time of 67μs which was not sufficient for the lamp used in this example. Hence the minimum burst time was increased to 6 lamp cycles.

$$\text{Digital Dimming Ratio} = (60\text{kHz}/100\text{Hz})/(2 + 4) = 100:1 \quad (\text{Eq. 2})$$

In Figure 3, the device's analog dimming capability was used to extend the dimming ratio to approximately 300:1 since each device can reduce the lamp current by up to one-third.

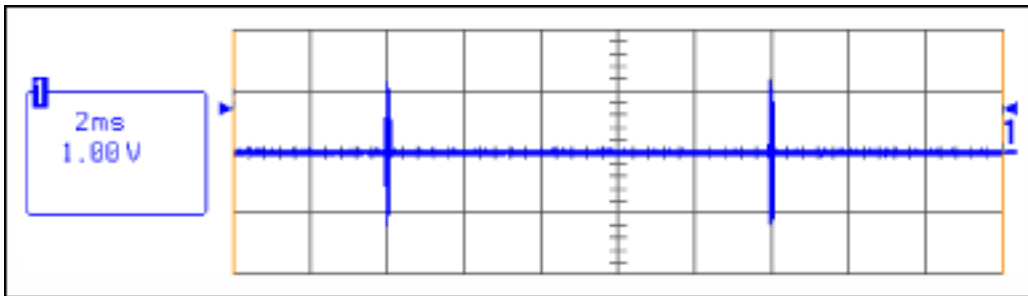


Figure 1. Lamp current at minimum PWM burst.

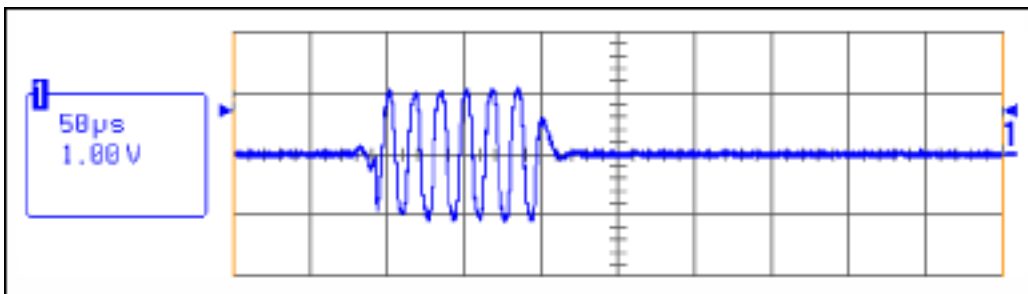


Figure 2. Lamp current at minimum PWM burst and nominal lamp current.

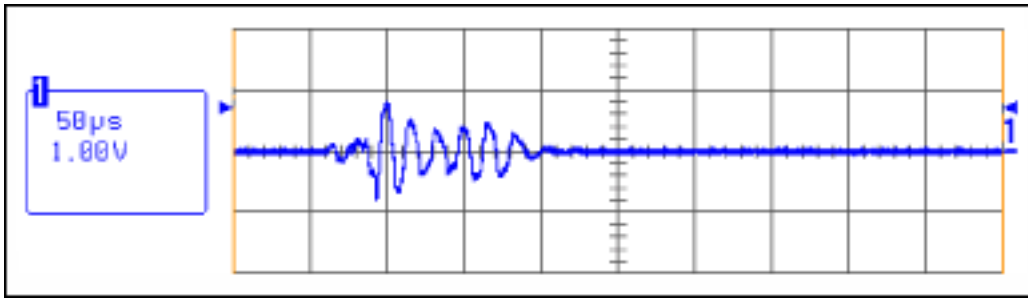


Figure 3. Lamp current at minimum PWM burst and minimum lamp current.

Dynamic Light Brightness Changes at Low Dimming Levels

The human eye can detect relative step changes in light that exceed about 20%. In applications using digital burst dimming, at the minimum burst there may only be 4 lamp cycles. Moving up from 4 lamp cycles to 5 lamp cycles can result in a relatively large step change in lamp brightness, a change which the user might see.

This undesirable brightness effect can be eliminated if analog dimming is used in conjunction with the digital dimming. For example, instead of increasing from 4 to 5 lamp cycles with the same analog current level, a preferable method creates an intermediate step in which the analog lamp current is increased before the move to the 5 lamp cycles. This intermediate adjustment will reduce the relative change in lamp brightness.

A similar article was published on the *CMP Industrial Control Design Line*, October 20, 2007.

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