



APPLICATION NOTE 399

DS31256 Loopback Modes

Abstract: This application note shows how to configure various loopback modes of the DS31256 HDLC controller, and how to verify and troubleshoot as necessary.

Introduction

This application note highlights the definition and functionality of the DS31256 loopback modes. These loopback modes can be used in channelized and unchannelized modes, depending on which mode has been configured for a given port. (Refer to Section 6 of the DS31256 data sheet.)

This application note does not cover the DS31256 configuration process. Please refer to the following application notes for configuration and initialization assistance.

- [App Note 2867: Initialization Steps for the DS31256](#)
- [App Note 2871: DS31256 HDLC Controller Step-by-Step Configuration—Configuration Mode](#)
- [App Note 2872: DS31256 HDLC Controller Step-by-Step Configuration—Bridge Mode](#)

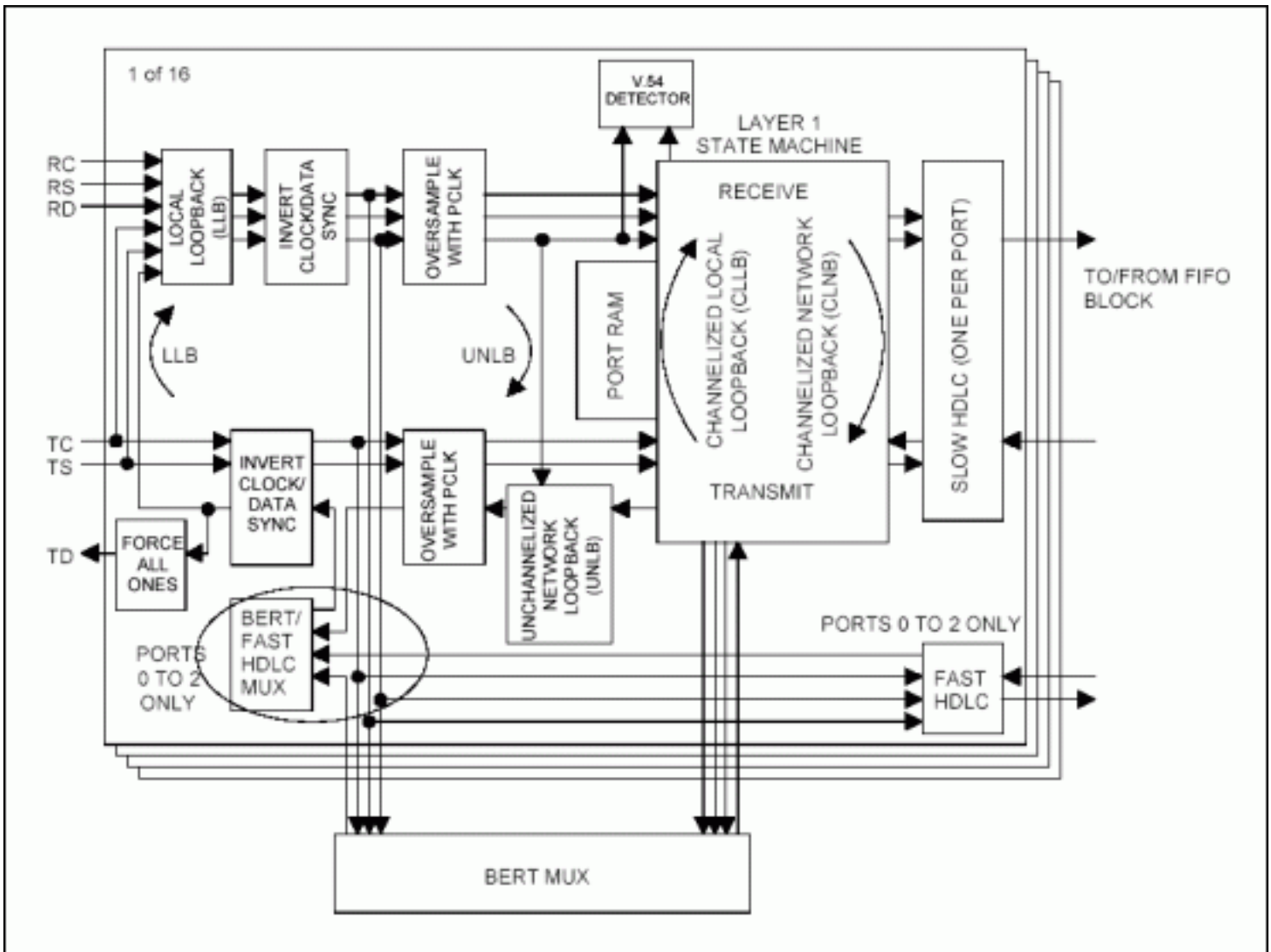


Figure 1. Layer 1 block diagram.

Loopback Modes

The DS31256 can be configured for local loopback mode or network loopback mode.

Local Loopback: In local loopback mode, loopback is internal to the DS31256. The data goes through the whole chip during the transmit and receive processes.

Network Loopback: In network loopback mode, loopback is done only in the Layer 1 block. The data is never written out to the host memory.

As shown in **Figure 1**, there are four different types of loopback that can be used in channelized and unchannelized modes.

LLB (Local Loopback Enable)

OFFSET/ADDRESS	NAME	FUNCTION	DATA SHEET SECTION
01xx	RP[n]CR	Receive Port n Control Register	6.2

LLB (Bit 10): This loopback routes transmitted data back to the receive port. It can be used in channelized and unchannelized port operating modes, including ports 0, 1, and 2, operating at speeds of up to 52MHz. The

receive clock input to the DS31256 is ignored by the chip after the local loopback is enabled (if the receive clock is provided).

UNLB (Unchannelized Network Loopback Enable)

OFFSET/ADDRESS	NAME	FUNCTION	DATA SHEET SECTION
02xx	TP[n]CR	Transmit Port n Control Register	6.2

UNLB (Bit 10): This loopback routes received data back to the transmit port. It cannot be used for port 0 to 2 operating in high-speed mode.

The other two loopback modes are accessed indirectly through the channelized port register data (CP[n]RD) register. The host must first write to the channelized port register data-indirect select (CP[n]RDIS) register to choose which channel and channelized port RAM it wishes to configure or read. On power-up, the host must write to all the used R[n]CFG[j] and T[n]CFG[j] locations to make sure they are set into a known state.

CLLB (Channelized Local Loopback Enable)

OFFSET/ADDRESS	NAME	FUNCTION	DATA SHEET SECTION
N/A	R[n]CFG[j] n = 0-15 Port j = 0-27 DS0	Receive Configuration	6.3

CLLB (Bit 10): Enabling this loopback forces the transmitted data to replace the received data. This bit must be set for the selected channel that is to be looped back. For the loopback to become active, the channel must be enabled (RCHEN = 1), and the channel must be set into the 64bps mode (R56 = 0).

CNLB (Channelized Network Loopback Enable)

OFFSET/ADDRESS	NAME	FUNCTION	DATA SHEET SECTION
N/A	T[n]CFG[j] n = 0-15 Port j = 0-27 DS0	Transmit Configuration	6.3

CNLB (Bit 11): Enabling this loopback forces the received data to replace the transmitted data. This bit must be set for the selected channel that is to be looped back. This bit overrides TBERT, TFA0, and TCHEN.

Troubleshooting

To determine and verify the cause of loopback problem, use the following information to help narrow down the debugging process.

1. Use the sequences and detailed information from the application notes listed at the beginning of this application note to initialize and configure the DS31256.
2. Check hardware such as the cable connection, or use the network loopback mode to test the device interconnections.
3. Invert only one of port clocks, either TP[n]CR.TICE, RP[n]CR.RICE. When local loopback is enabled on a high-speed unchannelized port, a data-sampling problem can occur, depending on the port clock frequency. This is because the propagation delays of the clock and data signals within the chip are aligning in such a way as to cause the data to be sampled while it is not stable. The problem can be

- corrected by inverting the port clock that shifts the data sample point by half a port clock cycle.
- Switching the DS31256 into local loopback mode can cause garbage to be received. Allocate enough buffers to hold the transmitted data, including any possible garbage.
 - Garbage data in receive FIFO: Empty the done queue every time before the initial transmission. After the channel has been configured and enabled, it takes approximately 5 frame periods, or 625 μ s, for the DS31256's internal logic to complete the transition to the new configuration. Once this transition has completed, the HDLC channel can be placed in loopback mode.

After the local loopback mode is enabled, the garbage data may be written into the Rx FIFO, most likely in high-speed mode. Before sending data, the following steps should be followed to ensure the garbage has been cleared. Some errors are reported in SDMA register at the same time.

- Put buffers in the Rx-free queue.
- Wait for the DS3134/DS31256 to write out the garbage data.
- Process the Rx-done queue.

The first packets of the channel may be the garbage data. For example, consider a case where 10 packets of data are sent out and everything is correct after steps 1 to 3. There may then be more than 10 packets in the memory, but only the last 10 packets are valid. In that case, only the last 10 packets in the memory should be checked. They are the correct data.

Application Note 399: <http://www.maxim-ic.com/an399>

More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

Other questions and comments: <http://www.maxim-ic.com/contact>

Related Parts

DS31256: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

AN399, AN 399, APP399, Appnote399, Appnote 399

Copyright © by Maxim Integrated Products

Additional legal notices: <http://www.maxim-ic.com/legal>