



APPLICATION NOTE 3940

MAX8632 PCB Layout Optimization

Abstract: This application note outlines a clear printed-circuit-board (PCB) layout for implementing the MAX8632 integrated DDR power supply.

Overview of the MAX8632

The [MAX8632](#) integrates a synchronous-buck controller to generate V_{DDQ} main rail, a 3A high-speed low-dropout (LDO) regulator that can source and sink current to generate VTT bus termination, and a 15mA VTTR reference buffer. The buck controller drives two external n-channel MOSFETs to generate output voltages down to 0.7V from a 2V to 28V input. The LDO can sink or source up to 1.5A continuous and 3A peak current. The LDO was designed as a terminator for the DDR memory bus where fast transients can be expected. This requires a control loop with high bandwidth and a circuit to match.

Implementing a High-Speed VTT Circuit

Because the MAX8632 circuit must function in the presence of large fast-transient signals, stray components and PCB inductance can reduce performance. This is why C11, C12, and PGND1 are connected to C4A and C4B with the lowest possible inductance trace (i.e. short and wide). Note that power flows from V_{IN} to V_{DDQ} to VTT; then, it flows to PGND2, back to PGND1, and on to RTN. Only a very small chip bias current flows into the analog-ground leg. Voltage feedback for the V_{DDQ} output is sensed at the output terminal and GND. Even though GND is on the other side of the chip, it offers good reference sensing because GND has only one connection to power return and that connection is at the single point where GND and PGND2 meet (see **Figure 2**). Voltage sensing for VTT has the same basis as V_{DDQ} , and, with C11, C12, C4A, C4B connected together, this GND establishes the system reference ground at this point. VTTR (C6) should also use this as the reference ground. Furthermore, any testing should use this point as a reference, and a test point should be installed here for this purpose.

Because VTT must handle large fast transients, a linear control loop has been deployed in the MAX8632. While switching supplies offer good efficiency, their output inductor limits current slew rate. Current slew rate is limited even in linear circuits, but the slew limiter in this case is lead, and trace inductance is much smaller than a switching supply inductor. Hence, higher transient speeds can be achieved. This is important to keep in mind when laying out the circuit. Using a transconductance output (voltage-controlled current source) can reduce some of the problems that inductance presents. Using a current source as an output raises the output impedance, which has two advantages. First, with increased resistance, the time constant (L/R) for the inductor is reduced. Second, with a high enough output impedance, the second-order pole that is formed by the inductor-capacitor output can be reduced to a single-pole system. In current-mode switching systems, similar attempts are made to reduce the effect of the output inductor. Of course, a linear regulator does not have the efficiency of a switcher, but this is the price that must be paid for high speed.

One other advantage of a high-speed VTT circuit is that the local capacitor can be much smaller. During the time the control loop is ramping current up to meet the load requirements, the output capacitors must supply the load. Therefore, if the VTT driver has a higher current slew rate, the output caps can be smaller. In fact, with a $20\mu\text{F}$ output cap, 40mV of voltage tolerance, and a 3A peak load transient, we can solve for the slew rate using $C \cdot V = Q$ and knowing $Q = I \cdot T$.

$$C \cdot V = T \cdot I \quad (\text{Eq.1})$$

Or:

$$\frac{20\mu\text{F} \cdot 40\text{mV}}{3\text{A}} = 267\text{ns}$$

And slew rate equals:

$$\frac{3\text{A}}{267\text{ns}} = 11.3\text{A}/\mu\text{s}$$

Putting this into perspective, with DDR2 there is 0.9V ($1.8\text{V}-0.9\text{V}$) available from the V_{DDQ} rail to drive VTT. The maximum output inductance required to support this speed is calculated with the following equation:

$$\frac{Di}{Dt} \cdot L_{MAX} = V \quad (\text{Eq. 2})$$

L_{MAX} is 80nH .

This must comprise the trace inductance and the chip, including the bond wires, package, and return ground. In most cases, 80nH can easily be achieved by placing a return ground on the immediate layer under the VTT trace and the VTT output caps and by placing them close to the VTT driver.

Figure 2 provides a simplified layout to illustrate the multiple layers of a real system. In this diagram, power enters at V_{IN} and exits at V_{DDQ} and VTT. With the analog ground (GND) isolated from PGND1, most of the switching noise generated by Q1 and Q2 shows up at V_{IN} and RTN. PGND2 and GND are connected with a single point at PGND2, allowing GND to float on top of the DC errors and noise caused by ground currents.

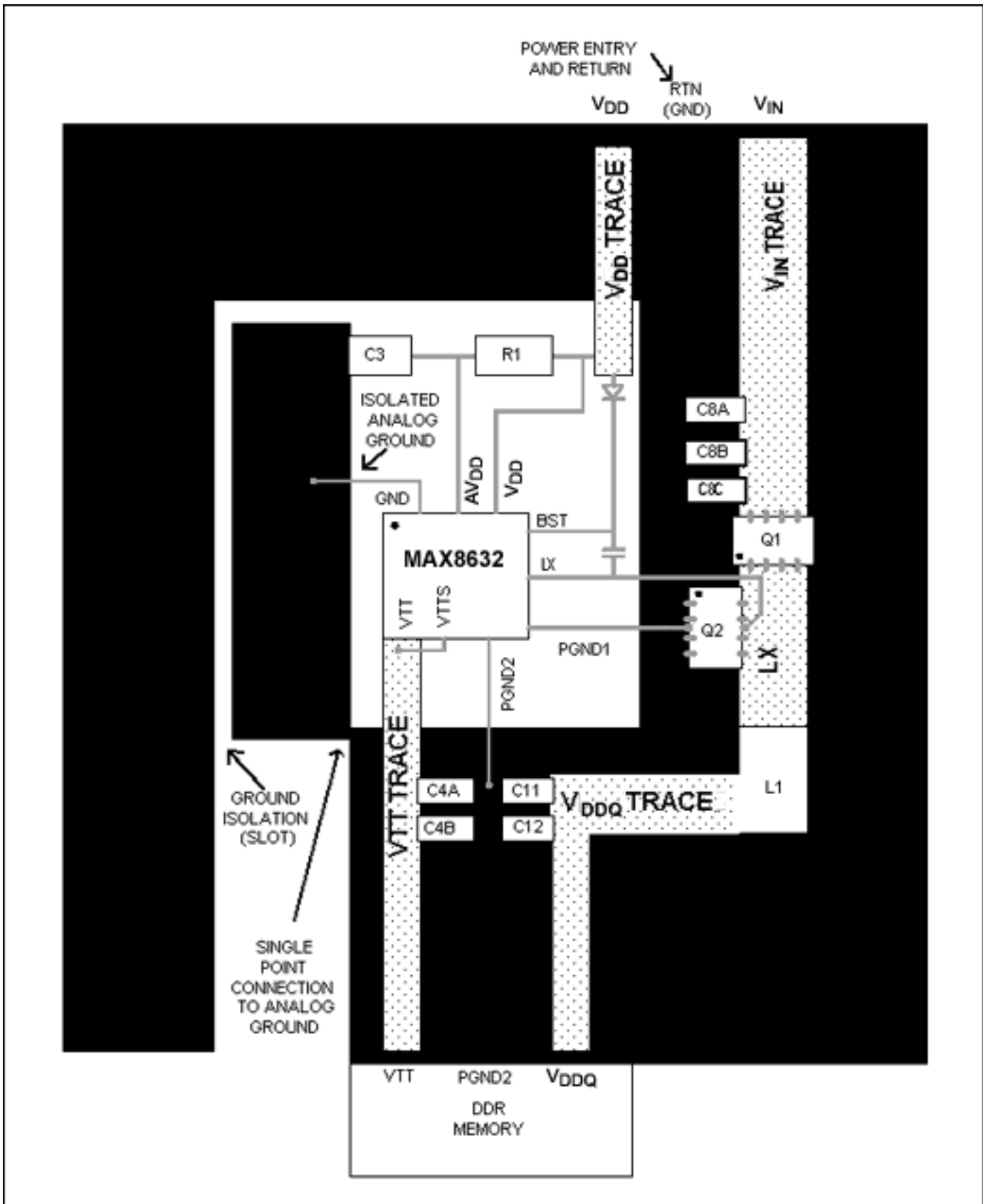


Figure 2. This is a simplified PCB layout for the MAX8632. Notice the isolated analog-ground patch and its single-point connection to PGND2.

A low-noise, 5V bias supply (AV_{DD}) is generated using a resistor-capacitor filter from the 5V V_{DD} input. R1 and C3 filter the noise generated by the boost circuit, and C3 is terminated into GND to reduce noise. R13 and C1 also filter supply noise (see **Figure 3**)—in this case, the ripple from V_{DDQ} . If the ripple from V_{DDQ} is forwarded to

VTT, the LDO will try to drive the 10 μ F output caps (C4A, C4B). With a 30mV V_{DDQ} ripple and a 300kHz switching frequency, as much as 90mA of current is needed to drive the VTT caps. Because the V_{DDQ} regulator can skip pulses (SKIP), there is less current at light loads. The 80kHz filter formed by R13 and C1 reduces this current to 18mA and, at the same time, allows VTT to dynamically track V_{DDQ} .

Phase Margining

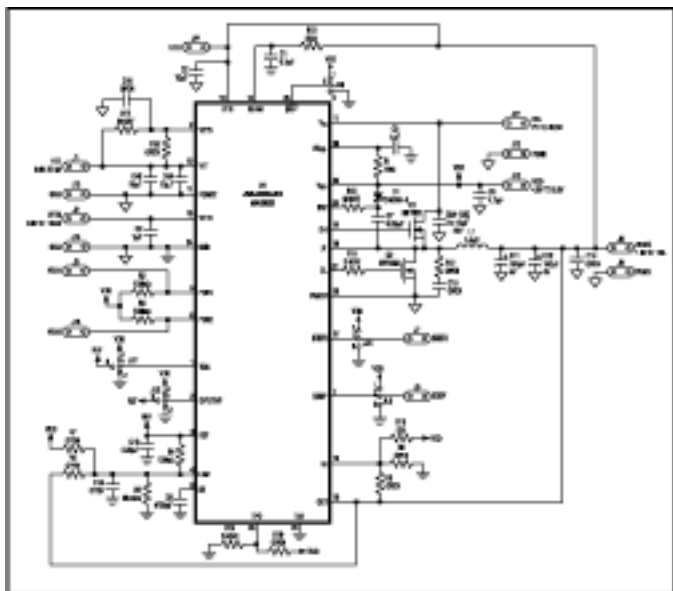
Although the VTT circuit should have sufficient phase margin by moving the feedback point inboard, extra phase margin can be found. This is because some lead phase shift is seen on the lead and trace inductance feeding the VTT output caps. On the other hand, if the feedback point is on the VTT output caps (outboard sensing) some phase margin is lost, but better sensing of output transients and DC accuracy is gained. This configuration allows the circuit to be tuned for optimum performance. The MAX8632 EV Kit has jumper-selectable VTT feedback, which can be seen in the Figure 3 schematic where R16 and R17 select an inboard or outboard feedback point.

Heat Dissipation

The MAX8632 has an exposed pad to help transfer heat from the silicon wafer to the PCB. This metallic exposed pad does not have any electrical connection to the internal circuit. Keeping in mind that the exposed pad must conduct up to 2.68W, it can be tied to any ground. Tying the exposed pad to GND makes a convenient connection to PGND2 and GND (see **Figure 5**). The middle and bottom planes also connect to the exposed pad (**Figures 6, 7, and 8**). Notice both that the isolation slot in the ground planes separates PGND1 from GND and PGND2, and also where the grounds are forced to connect. With the ground planes connecting at the exposed pad, they can all conduct heat out of the chip.

Conclusion

Even though time, money, or board space may limit implementation of all the recommendations in this application note, it still offers a good reference design from which to begin.



[More detailed image \(PDF, 71.3kB\)](#)

Figure 3. The MAX8632 Standard EV Kit Schematic.

Table 1. The MAX8632 Evaluation Kit Bill of Materials

DESIGNATION	QTY	DESCRIPTION
C1	1	0.1 μ F, 10% 16V X7R ceramic capacitor (0603) Taiyo Yuden EMK107BJ104MA
C2, C4A, C4B	3	10 μ F, 10% 6.3V X5R ceramic capacitor (0805) Kemet C0805C106K9PAC or Taiyo Yuden JMK212BJ106MG
C3, C6	2	1 μ F, 10% 10V X5R ceramic capacitor (0603) TDK C1608X5R1A105K
C5	1	4.7 μ F, 20% 6.3V X5R ceramic capacitor (0805) TDK C2012X5R0J475M
C7, C10	2	0.22 μ F, 20% 16V X7R ceramic capacitor (0603) TDK C1608X7R1C224M
C8A, C8B, C8C	3	10 μ F, 20% 25V X5R ceramic capacitor (1210) Taiyo Yuden TMK325BJ106MM TDK C3225X5R1E106M
C9	1	4700pF, 50V X7R ceramic capacitor (0603) Kemet C0603C472K5RAC3946 equivalent
C11, C12	2	150 μ F, 4V 18m Ω POS capacitor Sanyo 4TPE150MI
D1	1	Schottky Diode, 30V, 100mA (SOD-323) Central CMDSH-3
JU1, JU2, JU3, JU4, JU6	5	3-pin header, 0.1in center Sullins: PTC36SAAN (available in a 36-pin strip; place on PCB per example provided)
L1	1	1.4 μ H, 15.5A, 2.8m Ω power inductor Sumida, CEP125-1R4MC-U
Q1	1	n-channel MOSFET 30V 12m Ω (SO-8) International Rectifier IRF7821
Q2	1	n-channel MOSFET 30V 4m Ω (SO-8) International Rectifier IRF7832
R18	1	0 Ω 5% resistor (0603)
R1	1	10 Ω 5% resistor (0603)
R13	1	20 Ω 5% resistor (0603)
R2, R3, R4	3	100k Ω 5% resistor (0603)
R5	1	36.5k Ω 1% resistor (0603)
NONE	5	Shunts JU1 (3), JU2 (1-4), JU3 (3-2), JU4 (1-2), JU6 (1-2); Sullins STC02SYAN
U1	1	Integrated DDR Power Supply MAX8632 (5mm x 5mm, 28-pin TQFN)

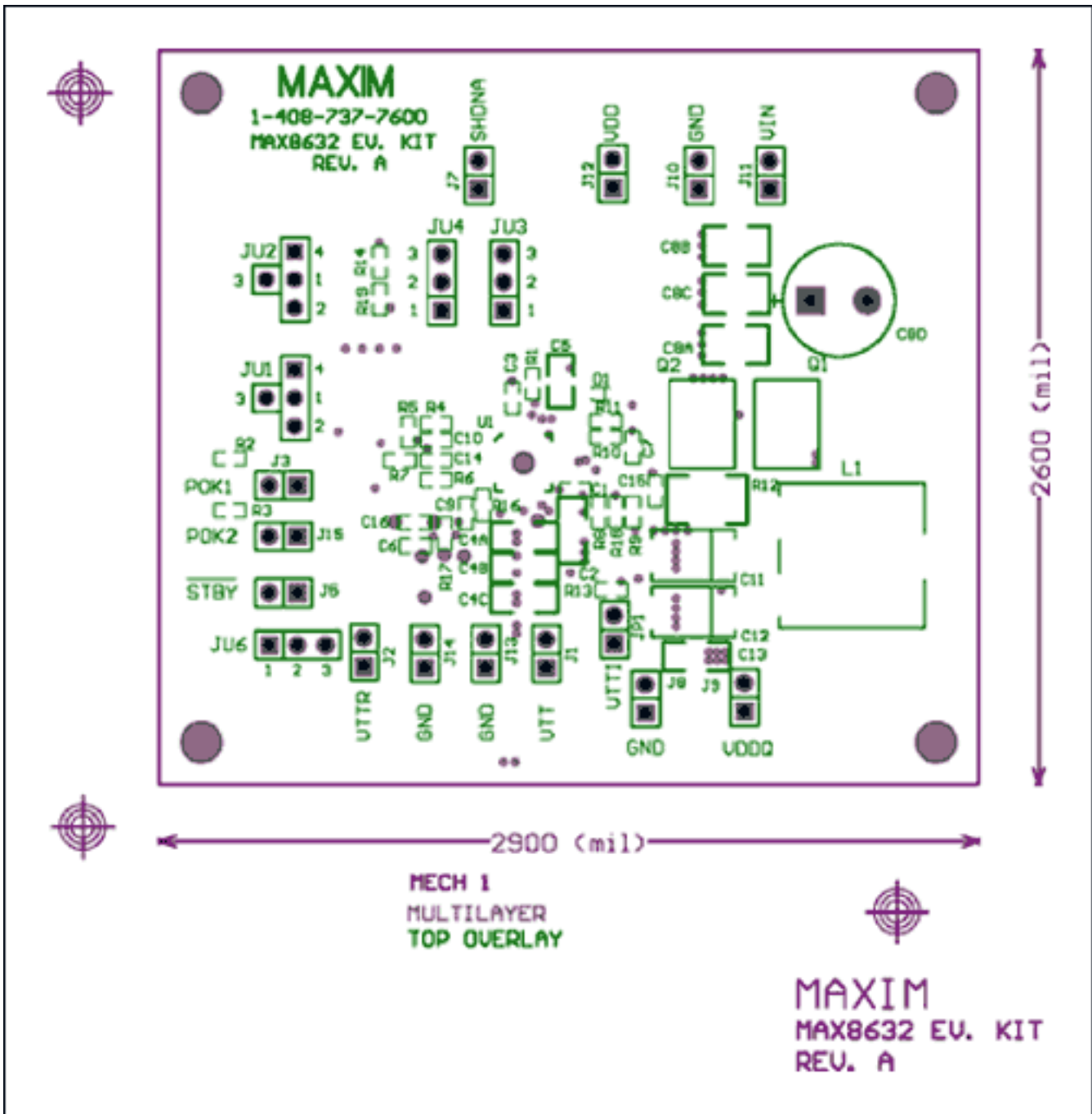


Figure 4. Top-side silk screen.

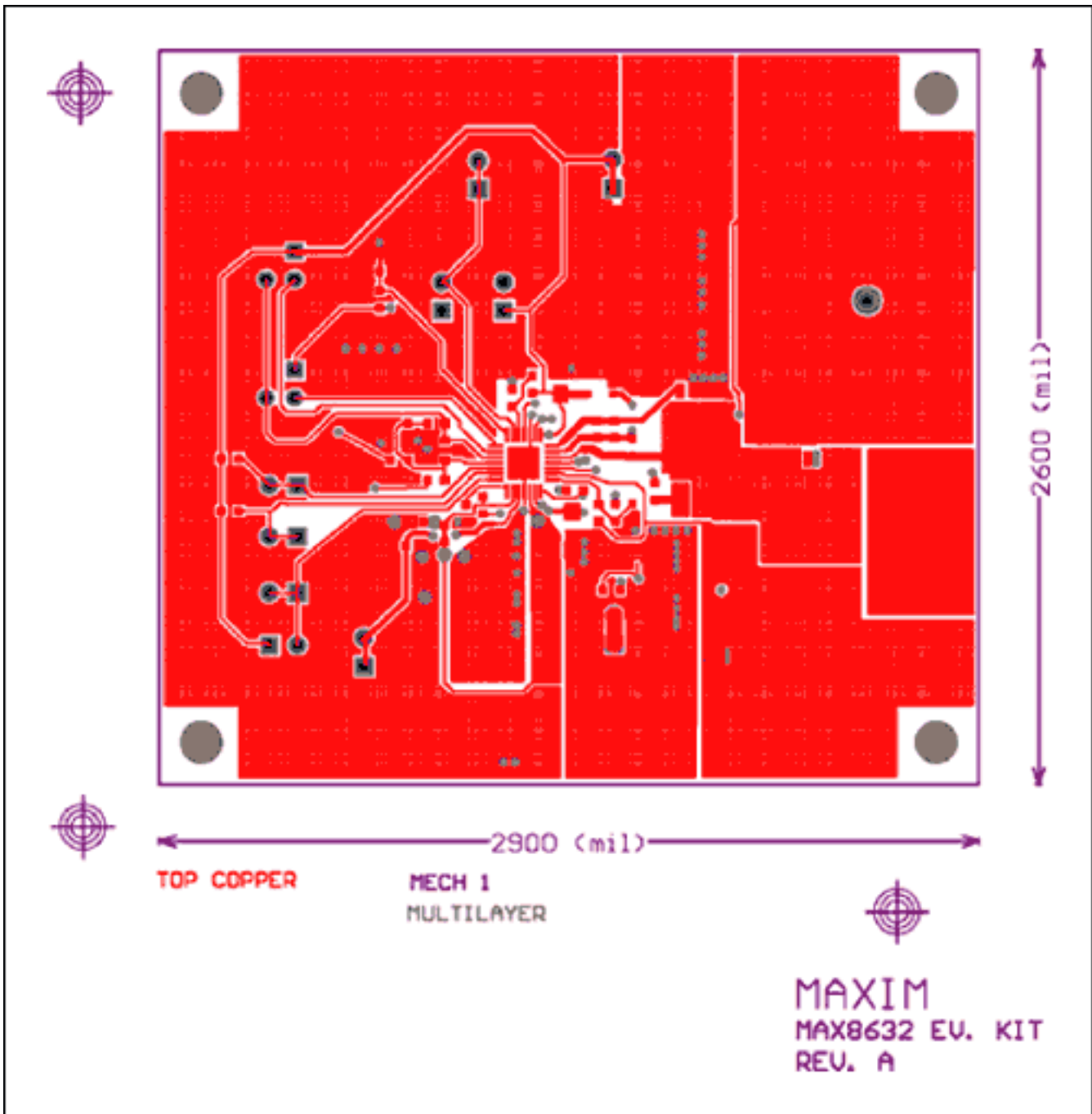


Figure 5. Top-side copper layout.

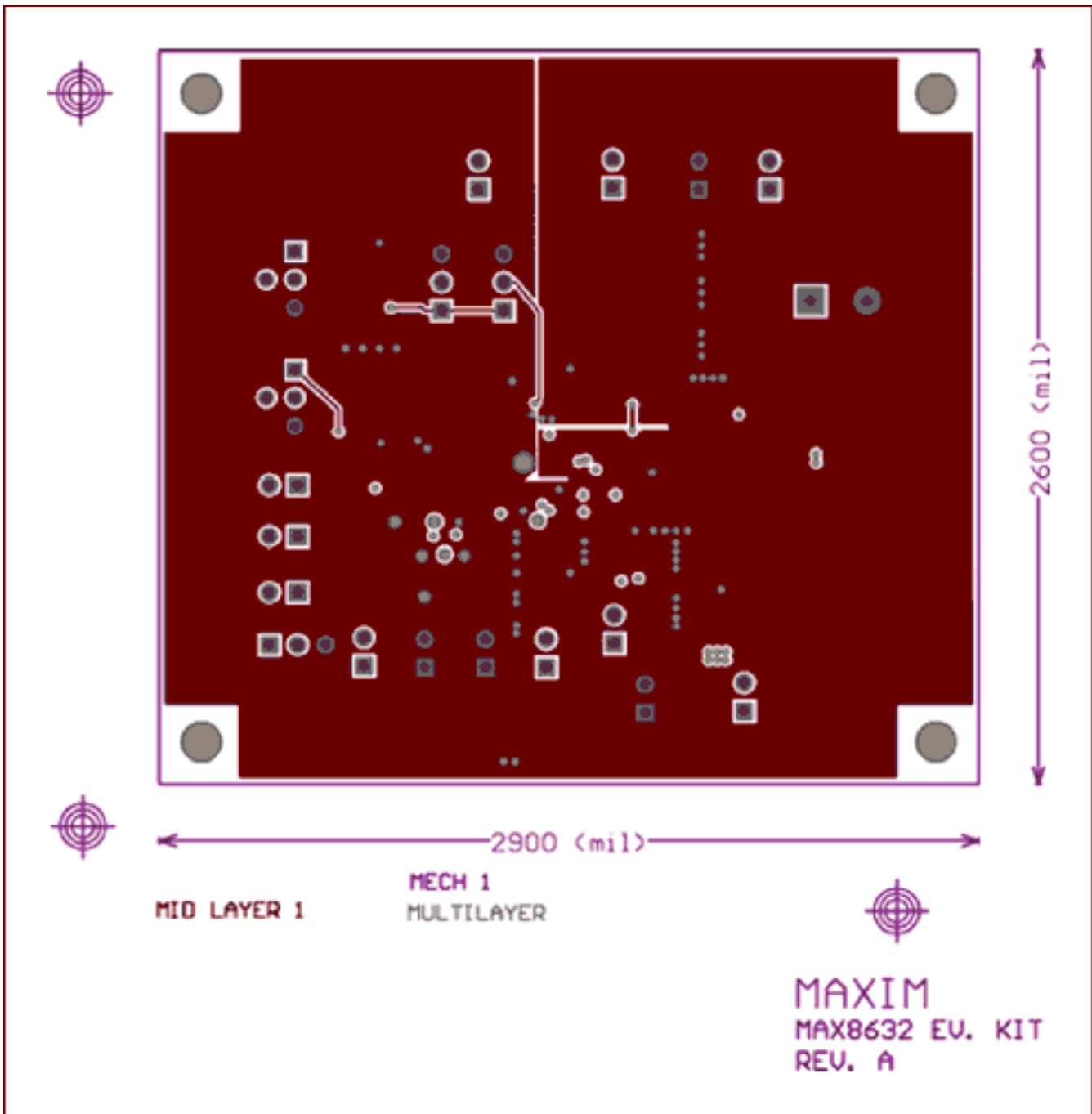


Figure 6. First middle copper layout.

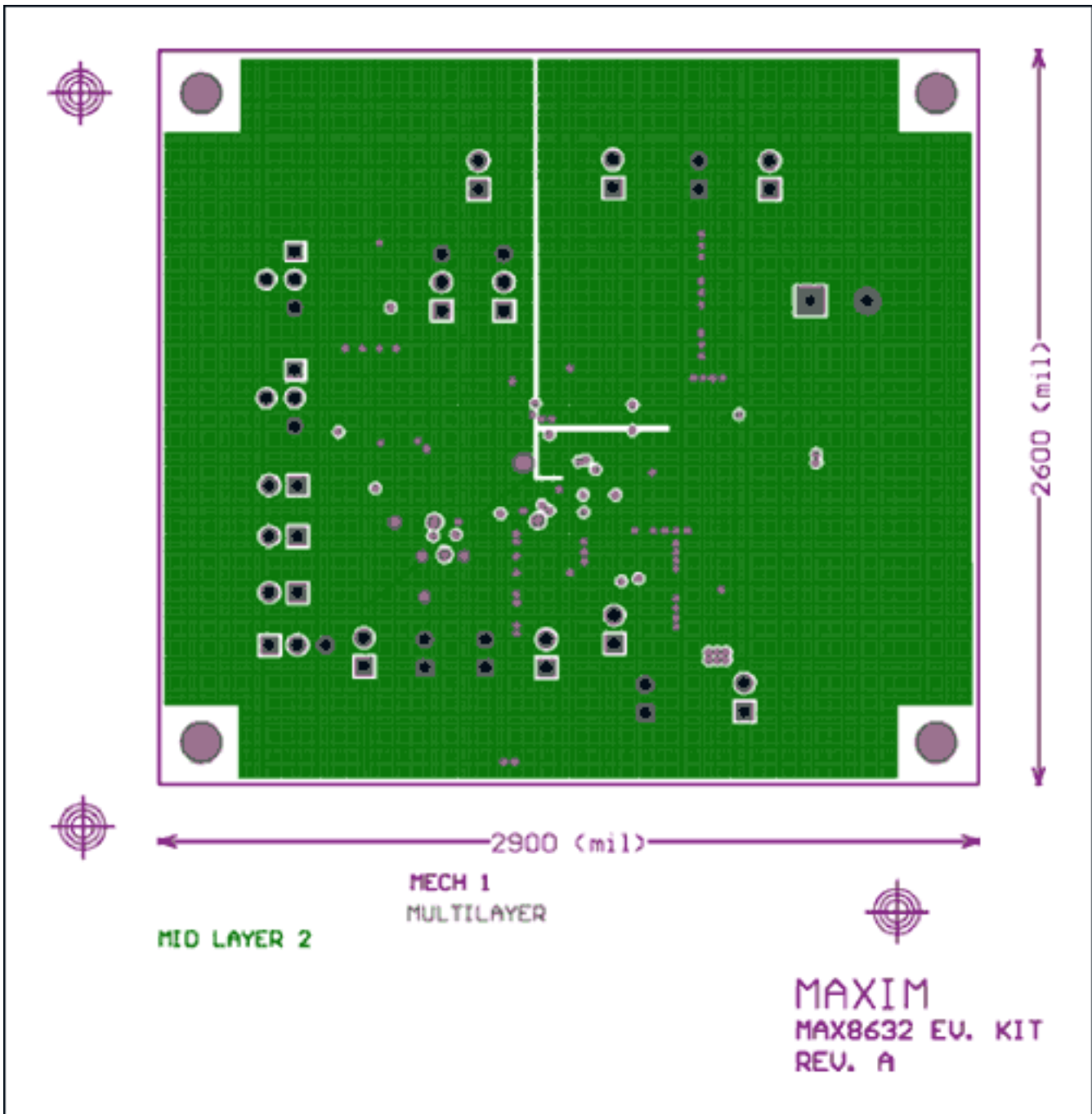


Figure 7. Second middle copper layout.

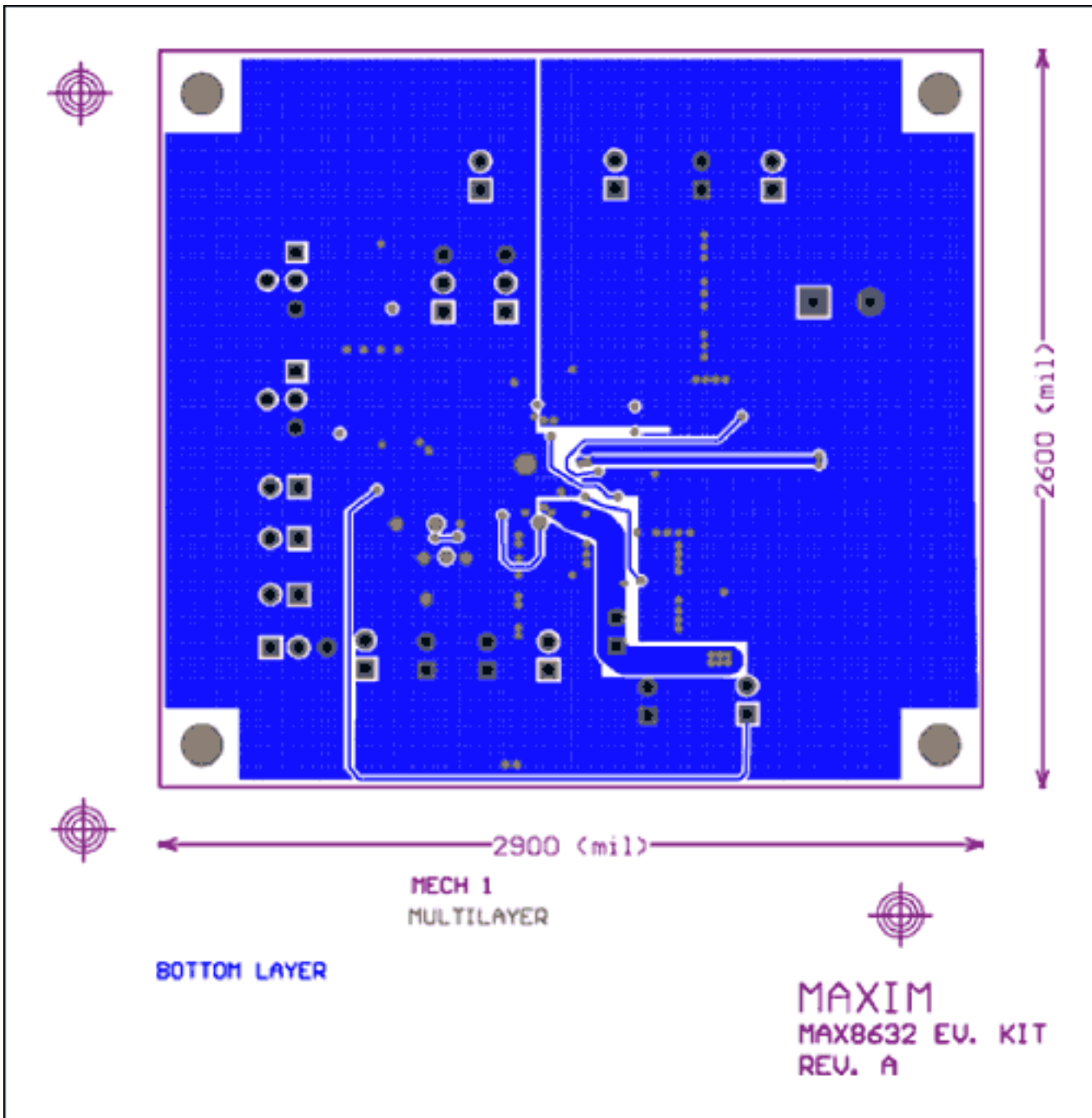


Figure 8. Bottom copper layout.

Application Note 3940: www.maxim-ic.com/an3940

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