

APPLICATION NOTE 3912

Low-Cost, Complete Power Solution for Powered Devices Includes a 12V Buck Converter

Abstract: The MAX5953A provides a simple and inexpensive, yet complete, nonisolated power solution for a powered device (PD) in a Power-over-Ethernet (PoE) system. The circuit provides the PD with detection and classification signatures in compliance with the IEEESM 802.3af standard, plus programmable inrush-current control, an integrated power switch, a PWM controller, and integrated high- and low-side switches. The buck step-down converter is capable of > 80% conversion efficiency while delivering 12V at 0.85A.

The circuit of **Figure 1** is the complete powered device (PD) with a DC-DC converter providing up to 0.85A at 12V. Although the MAX5953A contains both high- and low-side switching FETs, the internal low-side FET cannot be configured as a synchronous catch diode. Consequently, the buck converter uses only the high-side FET. Because the current-limiting circuit within the IC operates using voltage-drop information derived from current flow through the low-side FET, this circuit contains no automatic current limiting. The included fuse, F1, provides short-circuit protection at startup.

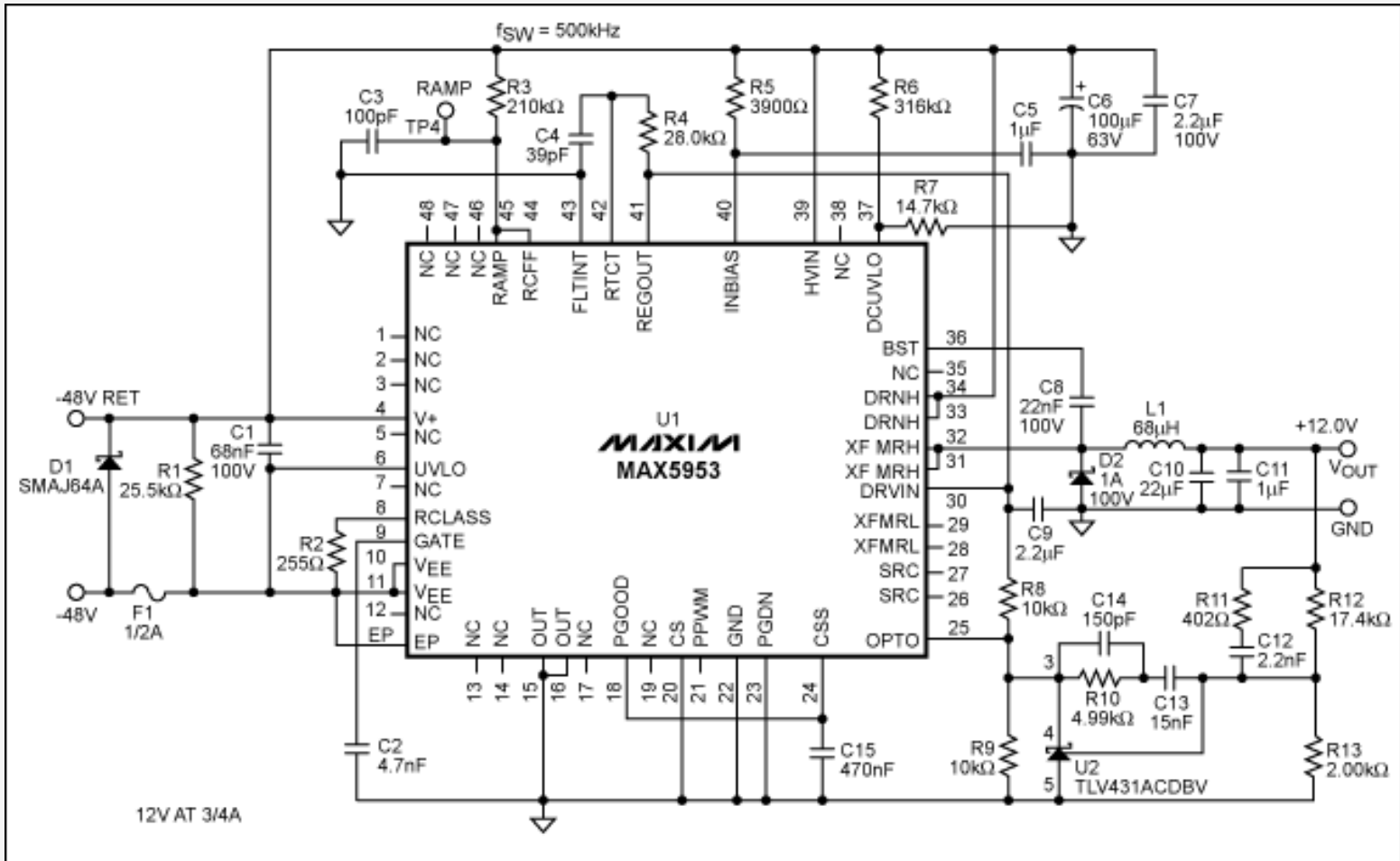


Figure 1. Schematic of the PD with a 12V, 0.85A buck converter.

The MAX5953A provides the following features:

1. TVS diode D1 protects against transient voltage spikes and against reverse-voltage application.
2. The circuit operates in three modes depending on the input voltage: PD detection signature, PD classification, and PD power. All voltage thresholds operate with or without the optional diode bridge, while complying with the IEEE 802.3af standard.

- In PD detection mode, the power source equipment (PSE) applies two voltages at V_{IN} in the 1.4V to 10.1V range with a minimum step of 1V, and records the corresponding current measurements at those two points. The PSE then computes $\Delta V/\Delta I$ to ensure the presence of the 25.5k Ω signature resistor, R1. Most of the MAX5953A's internal circuitry is off, and the offset current is below 10 μ A.
 - In classification mode, the PSE classifies the PD based on the power consumption required by the PD. Resistor R2 (255 Ω) signals the PSE that this PD will operate in Class 3 at a maximum power of 6.49W to 12.95W. Classification current is turned off when the device enters the power mode.
 - When V_{IN} rises above the 38V UVLO threshold, the MAX5953A enters the power mode and gradually turns on the internal MOSFET to limit inrush current.
3. When the slow turn-on is complete and $V_{OUT} - V_{EE} = 1.23V$, PGOOD goes to open-drain mode. The soft-start capacitor C15 charges from an internal 33 μ A pull-up current to provide a soft start of the DC-DC converter. The DC-DC converter is prevented from operating until $V_{OUT} = -30V$ (with respect to V_+), as set by resistor voltage-divider R6/R7 and the 1.33V DCUVLO threshold.
 4. Because the Class 3 power limit is 12.95W, the load is limited to 0.85A at 12V with a power conversion efficiency of 80%.

Hot-Swap Circuit Description

The default UVLO turn-on voltage is 38.6V, and the default turn-off voltage is about 30V. The UVLO turn-on and turn-off can be set to any value between 12V and 67V by connecting a resistor voltage-divider between V_+ and V_{EE} with tap at UVLO.

Once the UVLO is reached, an internal FET is slowly turned on by charging the FET gate with a 10 μ A current. This slow turn-on minimizes charging current of the 100 μ F C6. In this circuit, the hot-swap output voltage at OUT falls at a rate of $\approx 910mV/ms$, and the fall begins $\approx 8ms$ after voltage is applied at the input. See **Figure 2**.

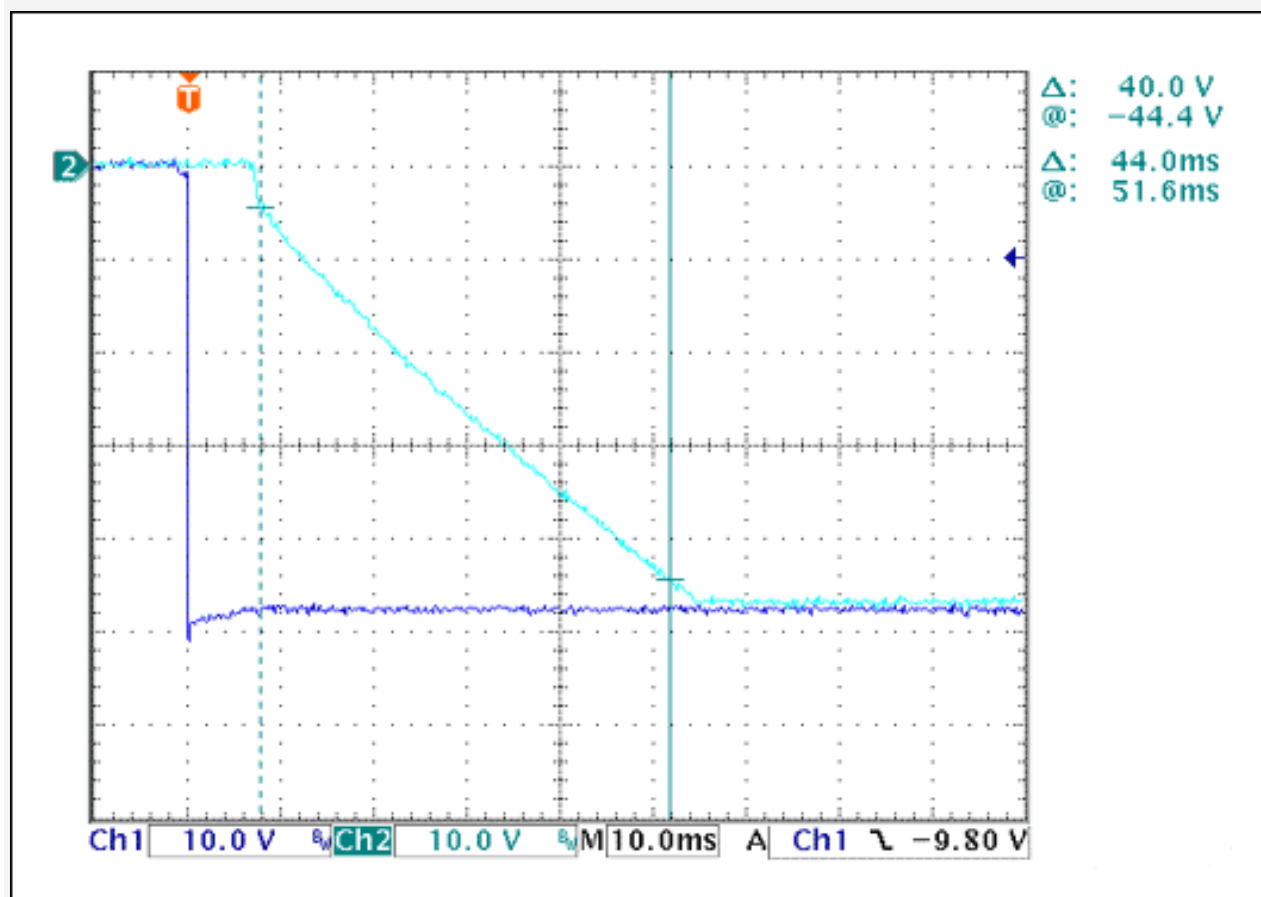


Figure 2. Hot-swap turn-on and ramp timing.

CH1 = V_{SS} , CH2 = V_{OUT}

PWM Circuit Description

The DC-DC converter is a typical buck converter that uses the internal high-side FET and an external Schottky catch diode. The operational input range is 30V (set by the resistive-divider at DCUVLO) to 60V. This range corresponds to a step-down ratio of

2.5:1 minimum to 5:1 maximum. The resultant duty cycle is 20% to 40%. The switching frequency is set to 532kHz by R4 and C4 to provide a minimum ON pulse width of $\approx 420\text{ns}$ to keep switching losses low.

Soft-start is provided by a combination of timing operations: by limiting the feedback voltage at OPTO to no more than 1.45V above the voltage at C_{SS} , and by charging the capacitor at C_{SS} by an internal $33\mu\text{A}$ current source. C_{SS} is initially clamped to GND by PGOOD, but PGOOD is released as the hot-swap function is completed when OUT is within 1.2V of V_{EE} . This procedure allows a slow ramp on the feedback signal at startup, slowly increasing the duty cycle to prevent output overshoot. The soft-start feature is apparent by the slope on the OPTO pin at startup (**Figure 3**), and the ramp becomes operational as V_{OPTO} reaches $\approx 2\text{V}$, as shown in **Figure 4** under high load and **Figure 5** under low load.

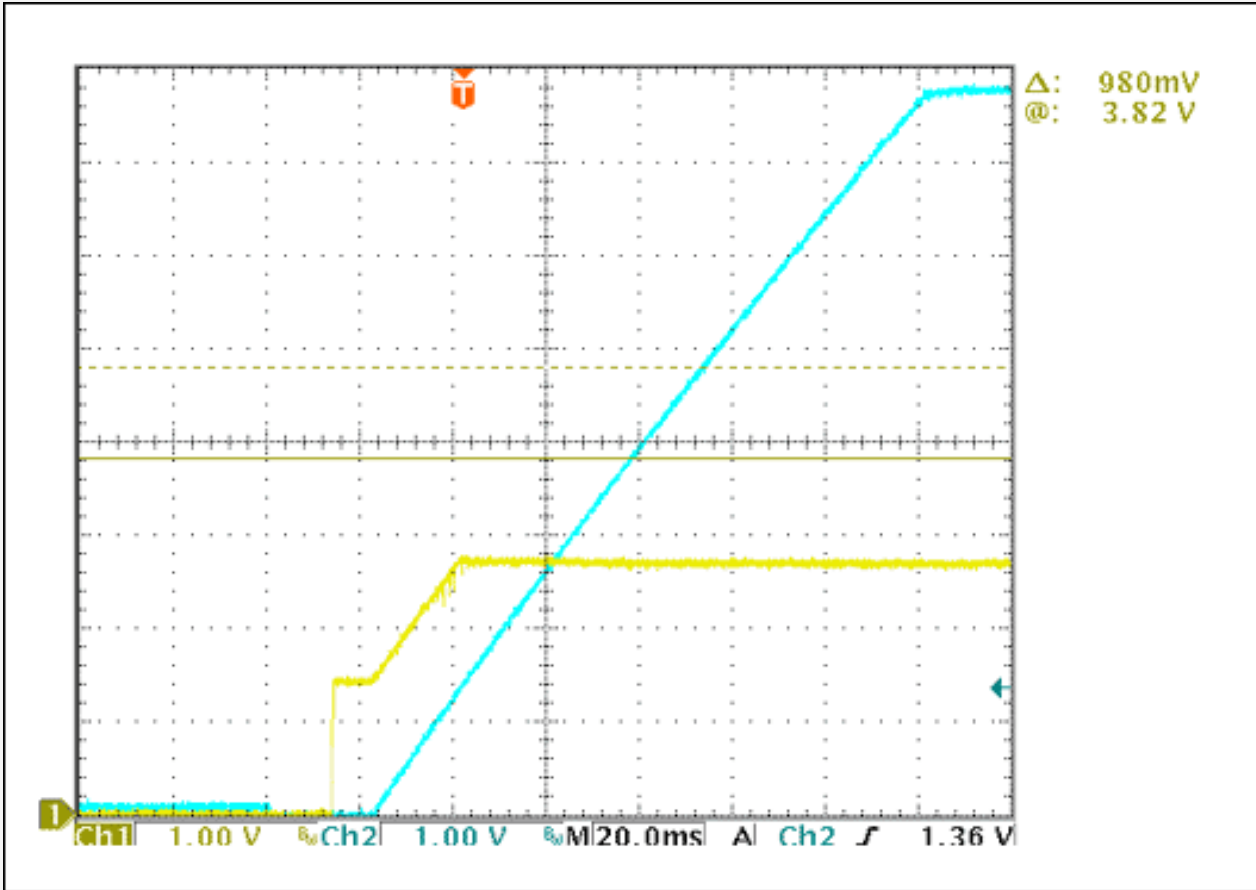


Figure 3. Soft-start timing.

CH1 = V_{OPTO} , CH2 = V_{CSS} ; $C_{SS} = 470\text{nF}$

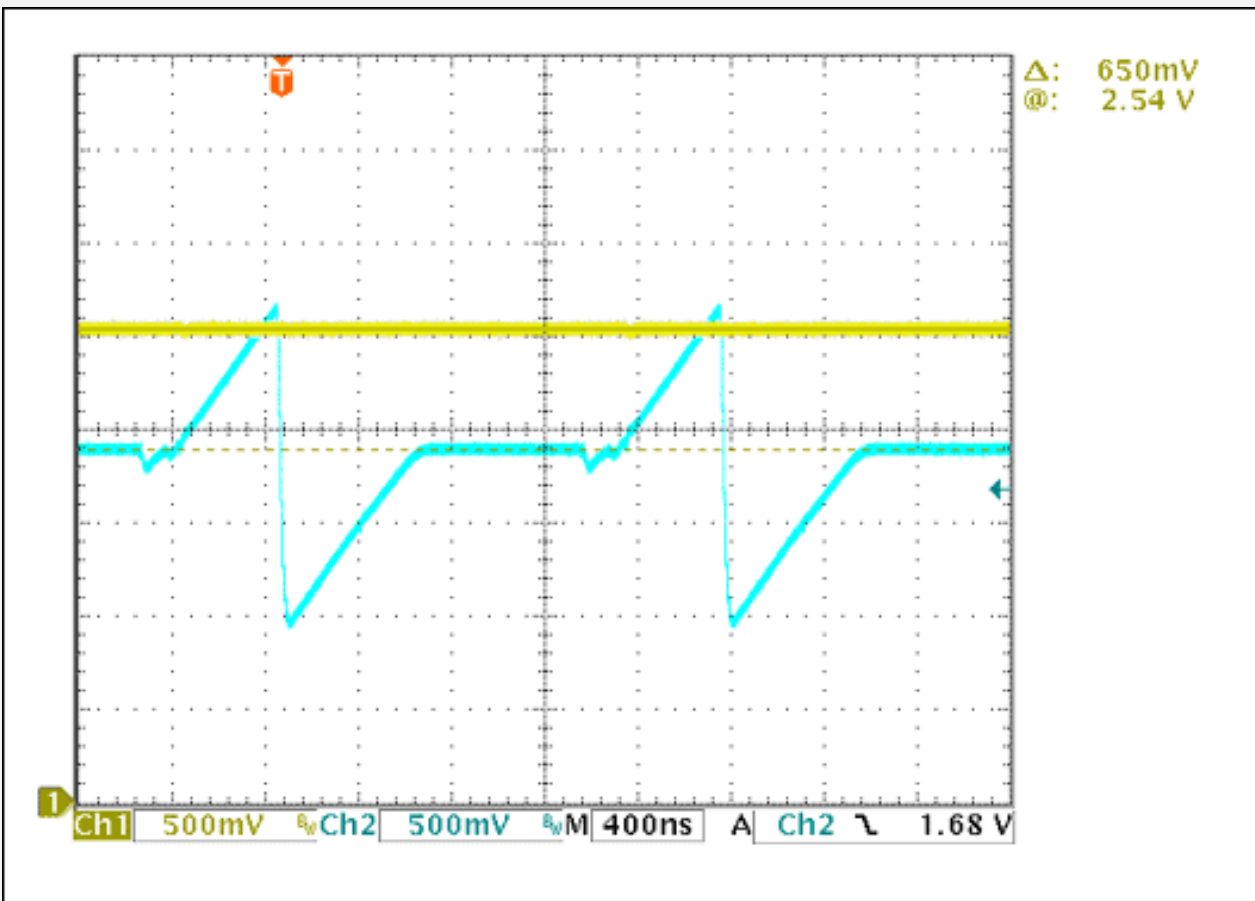


Figure 4. The PWM is controlled by comparing the feedback voltage at OPTO to the RAMP voltage.
 CH1 = V_{OPTO} , CH2 = V_{RAMP} , $I_{LOAD} = 400\text{mA}$

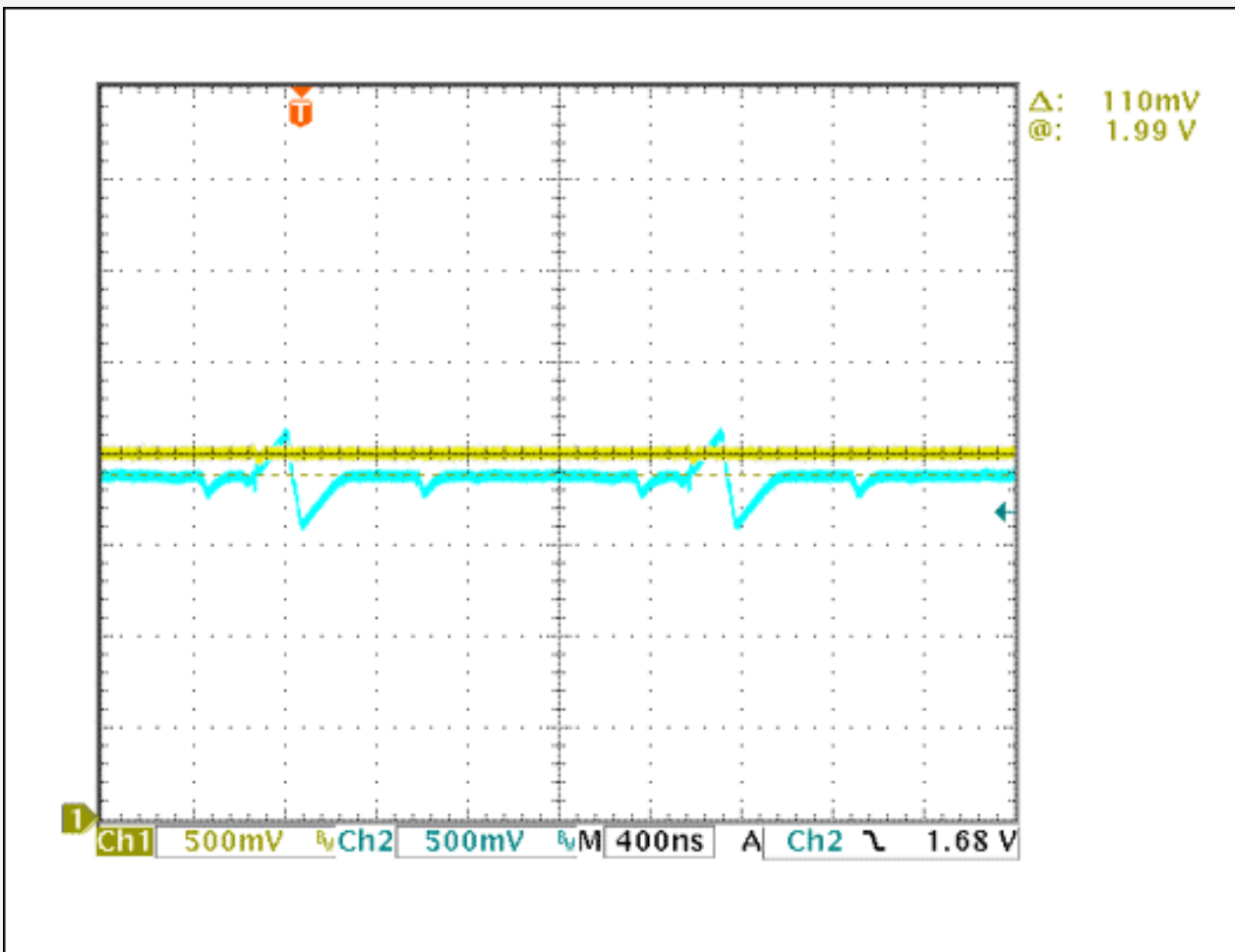


Figure 5. PWM ramp compared to the feedback voltage at OPTO under a low-current load condition.
 CH1 = V_{OPTO} , CH2 = V_{RAMP} , $I_{LOAD} = 50\text{mA}$

The controller operates in voltage mode with the voltage feed-forward ramp set by R3 and C3. The OPTO signal is compared with the voltage on RAMP.

Output-Voltage Overshoot at Startup

A soft-start capacitor (C_{SS}) value of 470nF minimizes overshoot to 1% or less, as shown in **Figure 6**. Lower C_{SS} values are only mildly effective in controlling output-voltage overshoot at turn-on, as shown in **Figure 7** where overshoot is 7.7% when $C_{SS} = 100\text{nF}$. Smaller C_{SS} values allow faster startup, but at the expense of increased output overshoot at turn-on.

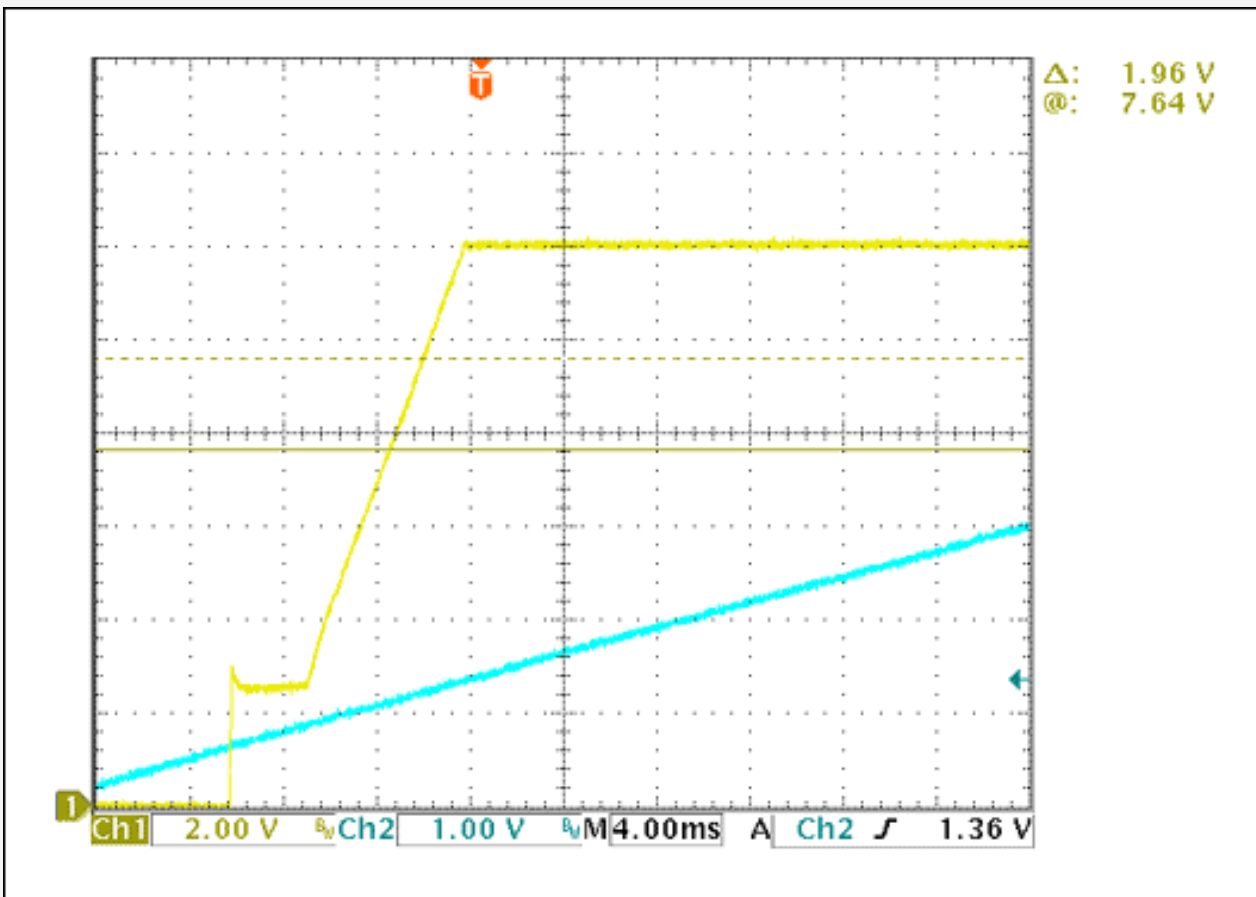


Figure 6. Startup output-voltage overshoot.

CH1 = V_{OUT} , CH2 = V_{CSS} , $C_{SS} = 470\text{nF}$, $R_{LOAD} = 30\Omega$ ($I_{OUT} = 400\text{mA}$ at 12V), Overshoot ≈ 0

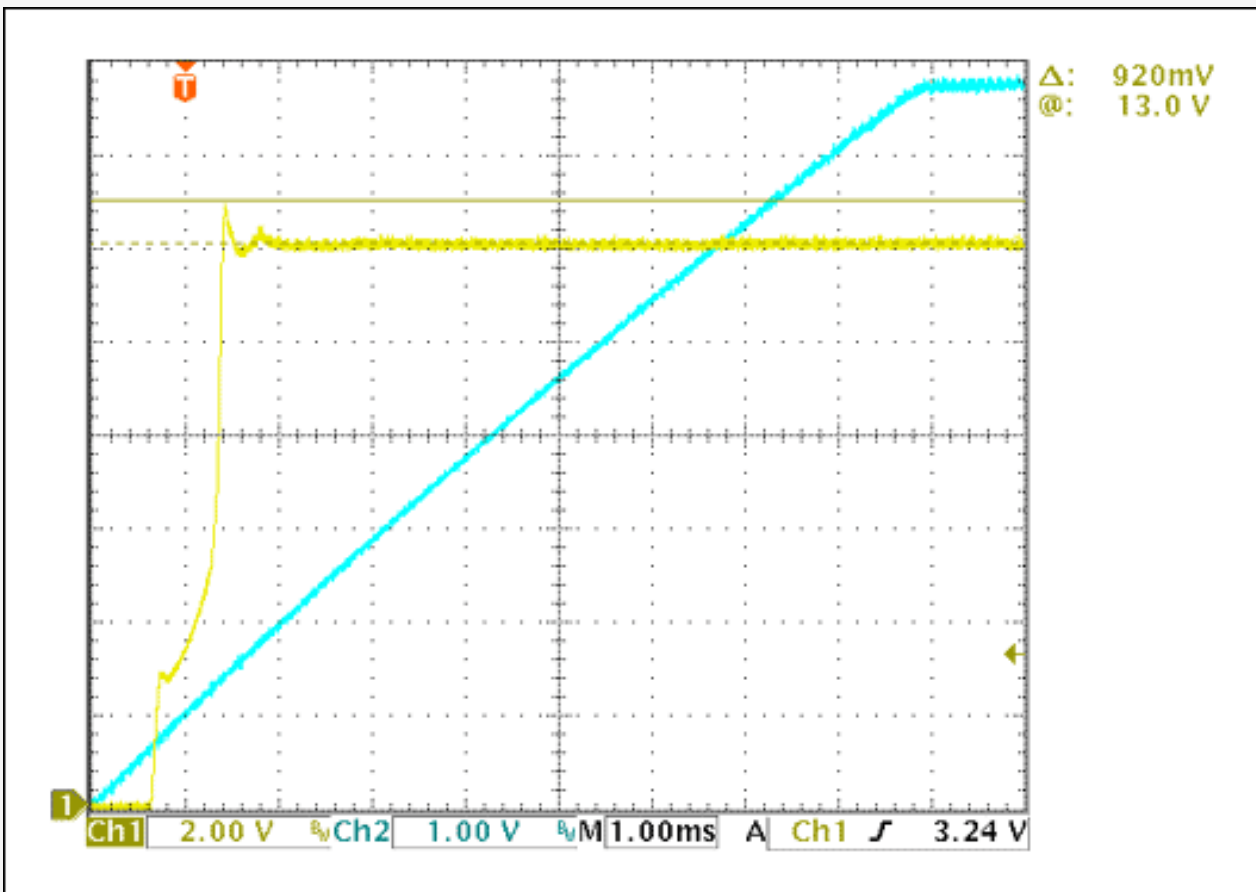


Figure 7. Output-voltage overshoot at startup.

$C_{SS} = 100\text{nF}$

Current Limiting

Although the MAX5953 integrates both high- and low-side FETs, the low-side FET is intended for transformer-coupled isolated forward or flyback circuits. The high- and low-side FETs are ON simultaneously, and current sensing is normally provided by sensing a voltage drop across the low-side FET. Because the low-side FET is not used, no current sensing is performed in this circuit. A fuse is provided to prevent damage to the MAX5953 and its internal pass FETs when a short circuit occurs. However, the fuse has limited effectiveness in protecting against output short circuits once the DC-DC converter has started. This is because the pass device may fail during the thermal time lag of the fuse.

Load Transients

Figure 8 shows load transients when switching between 1/2 load and full load. A fixed 400mA load is present, and a pulsed 400mA load is added in parallel at the output. If load is pulsed from 0mA to 400mA, as in **Figure 8**, the load transients increase considerably. However load transients are low, as shown in **Figure 9**, and are nearly independent of DC load current above 50mA.

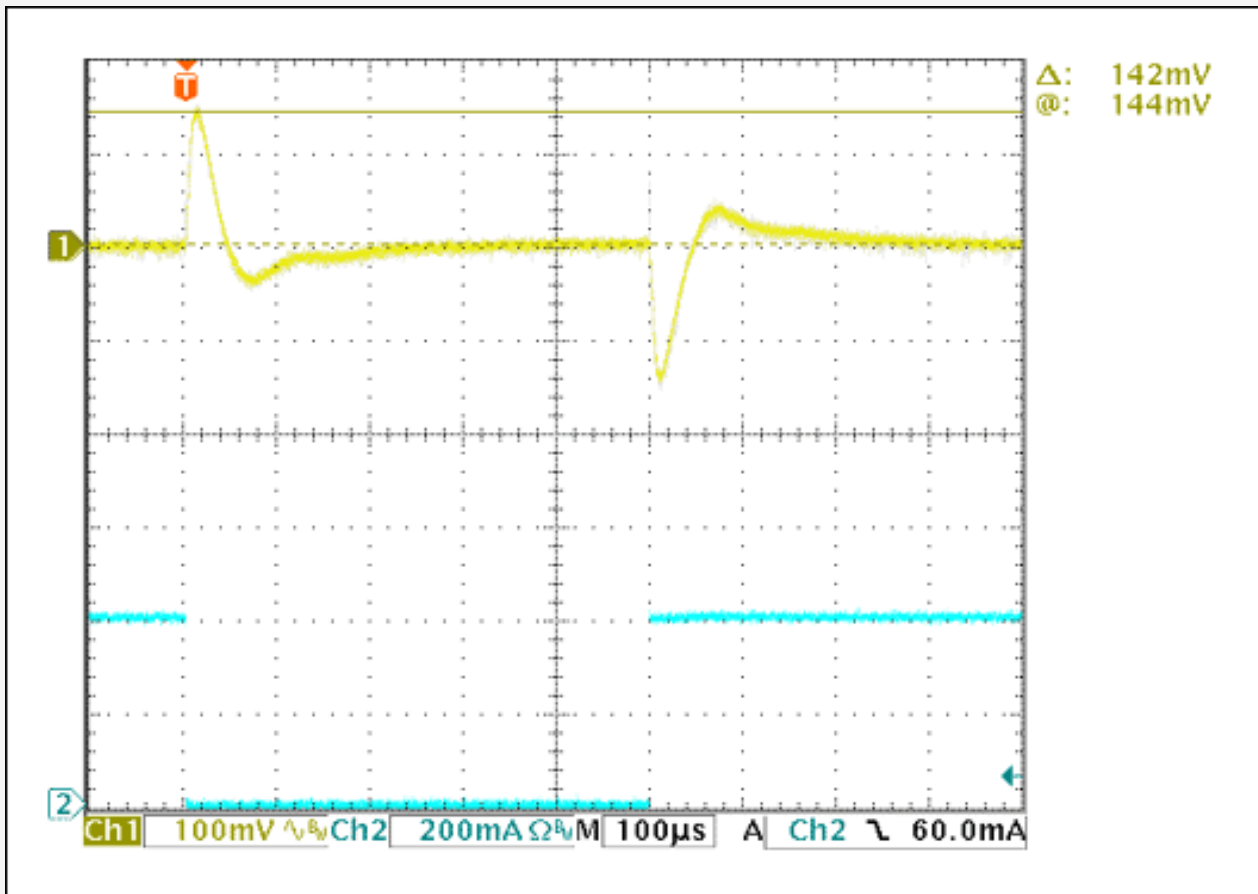


Figure 8. Load transients at 1/2 load to full load.

CH1 = V_{OUT} , CH2 = ΔI_{OUT} , Transients = 1.2%, $I_{OUT} = 800mA \rightarrow 400mA \rightarrow 800mA$

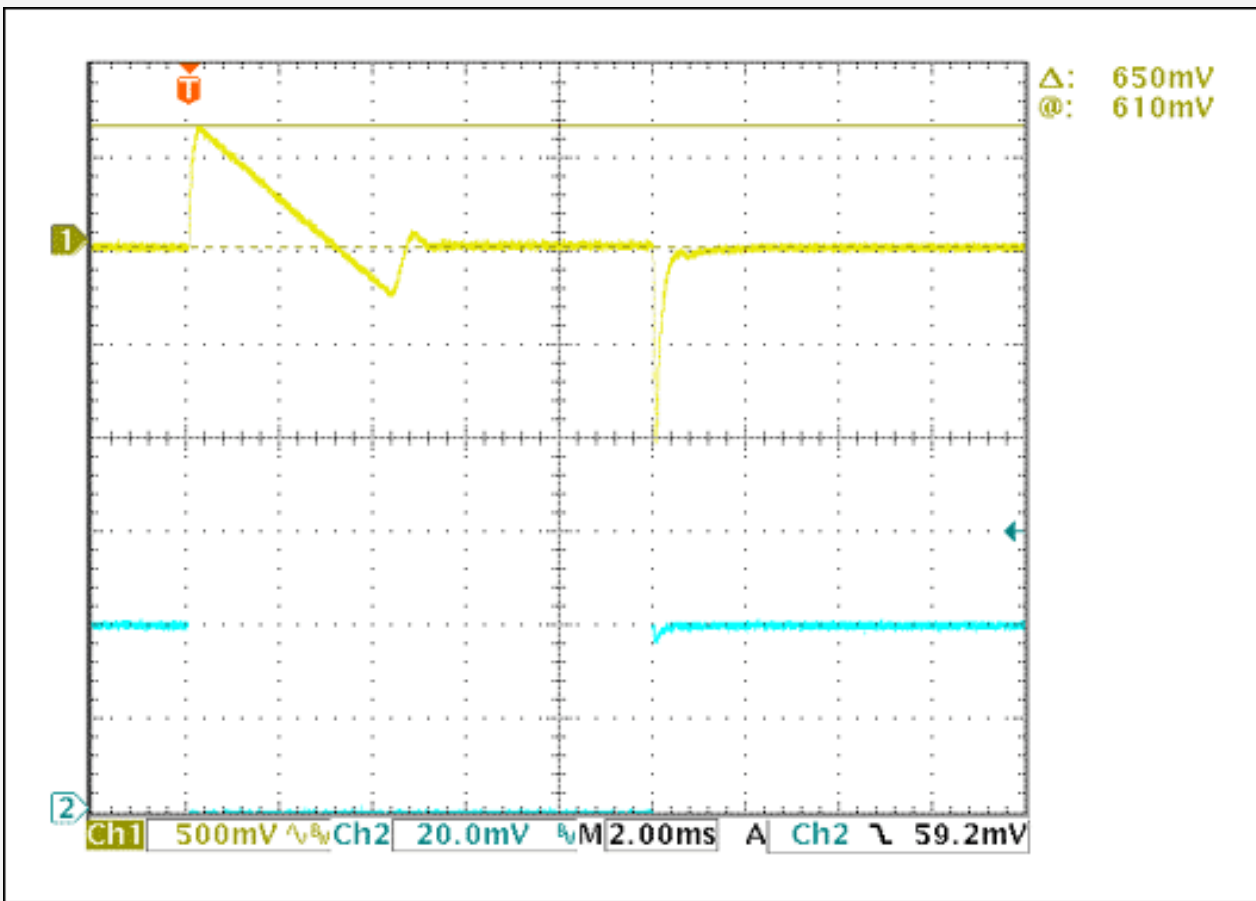


Figure 9. Load transients zero to 1/2 full load.

CH1 = V_{OUT} , CH2 = ΔI_{OUT} , Transients = 5% to 10%, $I_{OUT} = 400mA \rightarrow 0mA \rightarrow 400mA$

Conversion Efficiency

The conversion efficiency varies from 71% at 250mA load current to 80.5% at 1A load current. **Figure 10** shows that efficiency is > 80% at 850mA full load.

CONVERSION EFFICIENCY

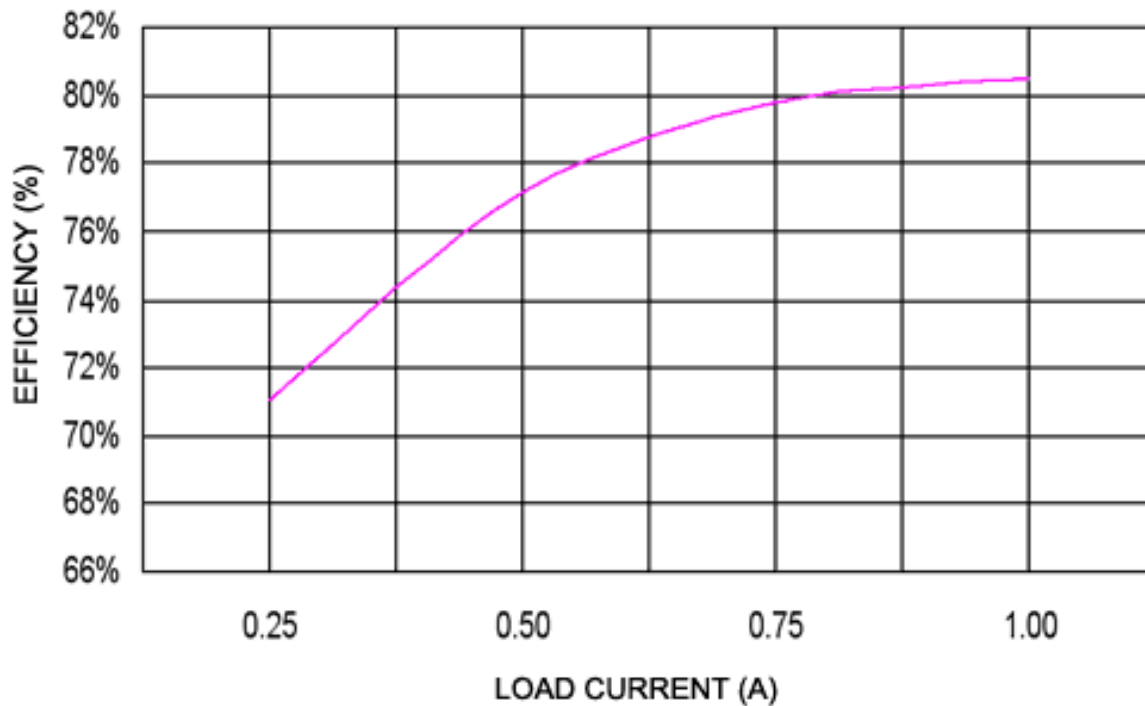


Figure 10. Conversion efficiency at $V_{IN} = 48V$.

Loop Stability

The voltage-mode control loop exhibits two poles at the 4.1kHz LC_{OUT} (L1, C9) resonance and a zero above 4MHz due to the small ESR of C_{OUT} . A type-3 loop compensation is used to allow a unity-gain bandwidth above the LC_{OUT} resonance. Two zeros are set at 2.1kHz (R9, C14) and 4.1kHz (R11, C15) to compensate for the double pole at the LC_{OUT} resonance. Two poles are placed at 20kHz (R9, C13) and 125kHz (R10, C15). The closed-loop Bode plot of the control loop in **Figure 11** shows a 19.4kHz unity-gain frequency with 59° phase margin.

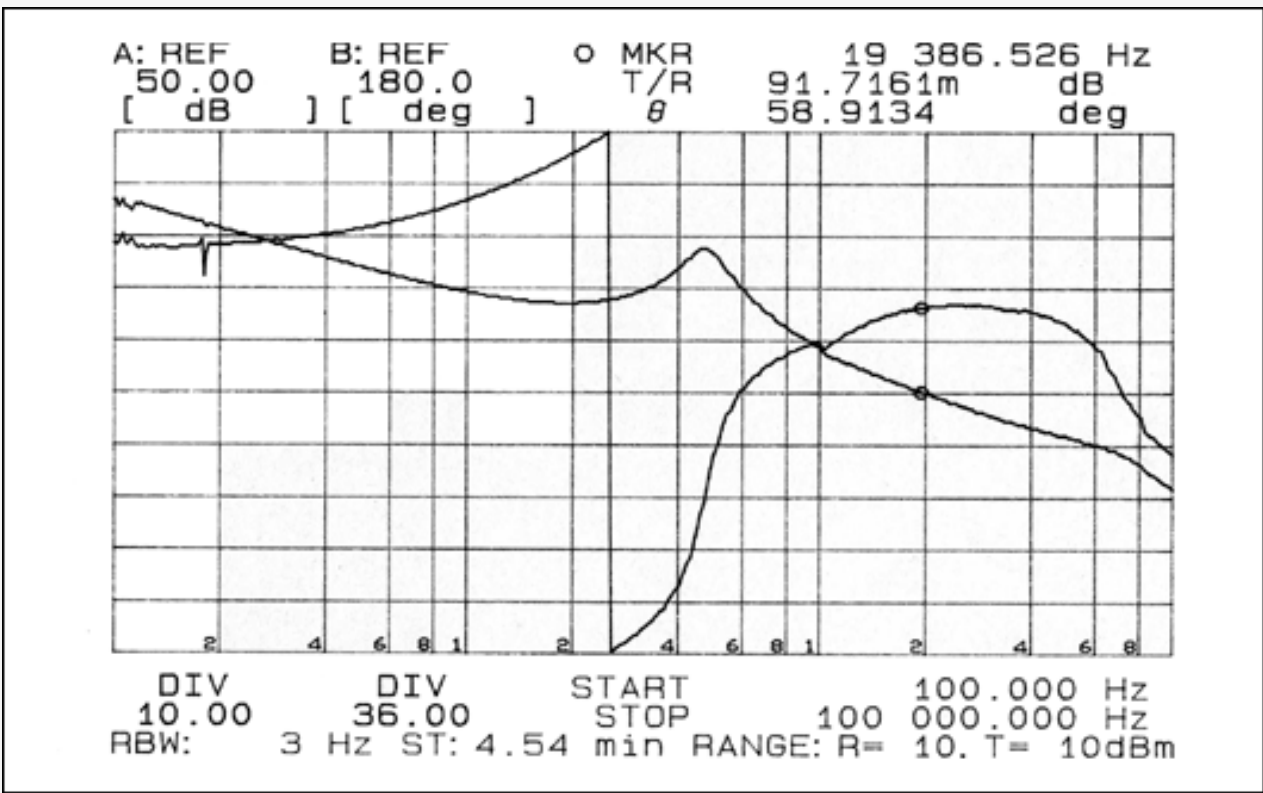


Figure 11. Closed-loop bode plot.

Application

This simple buck converter is most suitable in PD applications where its low-cost nontransformer-coupled structure outweighs the possible circuit failure under applied short-circuit conditions.

MAX5953A Bill of Materials

Qty	Description	Designator	Part Number
1	Capacitor, ceramic, X7R, 68nF, 10%,100V, 1206	C1	TDK C3216X7R2A683K Vishay VJ1206Y683KXB
1	Capacitor, ceramic, X7R, 22μF, 20%,16V, 1812	C10	TDK C4532X7R1C226M
1	Capacitor, ceramic, X7R, 1μF, 10%, 16V, 0805	C11	TDK C2012X7R1A105K
1	Capacitor, ceramic, X7R, 2.2nF, 10%, 25V, 0805	C12	TDK C2012X7R2A222K Vishay VJ0805Y222KXX
1	Capacitor, ceramic, X7R, 15nF, 10%, 25V, 0805	C13	TDK C2012X7R2A153K Vishay VJ0805Y153KXX
1	Capacitor, ceramic, NPO, 150pF, 5%, 50V, 0603	C14	TDK C1608COG1H151J Vishay VJ0805Y151JXA
1	Capacitor, ceramic, X7R, 470nF, 10%, 50V, 0805	C15	TDK C2012X7R2A474K Vishay VJ0805Y474KXA
1	Capacitor, ceramic, X7R, 4.7nF, 10%, 25V, 0805	C2	TDK C2012X7R2A472K Vishay VJ0805Y472KXX
1	Capacitor, ceramic, NPO, 100pF, 5%, 50V, 0603	C3	TDK C1608COG1H101J Vishay VJ0805Y101JXA
1	Capacitor, ceramic, NPO, 39pF, 5%, 50V, 0603	C4	TDK C1608COG1H390J Vishay VJ0805Y390JXA
1	Capacitor, ceramic, X7R, 1μF, 10%, 100V, 1210	C5	TDK C3225X7R2A105M
1	Capacitor, al. elec., 100μF, 20%, 80V, SM 10 x 10mm	C6	Panasonic EEV-FK1K1010
1	Capacitor, ceramic, X7R, 2.2μF, 20%, 100V, 1812	C7	TDK C4532X7R2A225M
1	Capacitor, ceramic, X7R, 220nF, 10%, 50V, 0805	C8	TDK C2012X7R1H224K Vishay VJ0805Y224KXX
1	Capacitor, ceramic, X7R, 2.2μF, 20%, 50V, 1210	C9	TDK C3225X7R1H225M
1	Diode, TVS, 64V, SMA	D1	Vishay SMAJ64A
1	Diode Schottky 90V, 1A , SMB	D2	ON Semi MBRS190T3
1	Fuse, 1/2A, 1206	F1	Littlefuse 0433.500
1	Inductor, 68μH, 1A, 10 x 10mm	L1	TDK SLF10145T-680M1R2
1	Resistor, thin film, 25.5kΩ, 1%, 0805	R1	
1	Resistor, thin film, 14.3kΩ, 1%, 0805	R10	
1	Resistor, thin film, 4.99kΩ, 1%, 0805	R10	
1	Resistor, thin film, 402Ω, 1%, 0805	R11	
1	Resistor, thin film, 17.4kΩ, 1%, 0805	R12	
1	Resistor, thin film, 2.00kΩ, 1%, 0805	R13	
1	Resistor, thin film, 255Ω, 1%, 1206	R2	
1	Resistor, thin film, 210kΩ, 1%, 0805	R3	
1	Resistor, thin film, 28.0kΩ, 1%, 0805	R4	
1	Resistor, thin film, 3.9kΩ, 5%, 0805	R5	
1	Resistor, thin film, 316kΩ, 1%, 0805	R6	
1	Resistor, thin film, 14.7kΩ, 1%, 0805	R7	
2	Resistor, thin film, 10.0kΩ, 1%, 0805	R8 R9	
1	IC, Controller, Power device +DC-DC converter TQFN50P700X700X48-EP	U1	MAX5953AUTM+
1	IC, Reference, 1.24V 1% SO-8	U2	TI TLV431ACDBV

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