

APPLICATION NOTE 3890

Using the DS28CZ04 in an Active Copper SFP Cable Assembly

Abstract: This document is a supplement to the [HFRD-16.0 reference design, 1Gbps to 4.25Gbps Active Copper SFP Cable Assembly](#). It shows how to use the DS28CZ04 as an SFP serial-control interface in active copper SFP cable assemblies. The reader is advised to obtain a copy of the reference design to understand details beyond the scope of this document.

Introduction

Network switches for Fibre-channel, Gigabit Ethernet, and InfiniBand™ operate at data transfer rates of 1Gbps and above. The standard interface for such equipment is the SFP port (small form-factor pluggable), which provides the same functionality as a regular GBIC (gigabit interface converter) but in a smaller and denser physical size. Active copper SFP cable assemblies plug directly into the SFP ports. Transceiver electronics built into the connector of such cables regenerates and conditions the signal for up to 20 meters in length between devices at 4.25Gbps. The **Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA)** ¹ defines the mechanical (physical dimensions) and electrical interface (pin assignment, protocol, etc.), including specification of the module definition interface and the data field descriptions. These plug-and-play data fields, also referred to as SFP Serial ID, are stored in an I²C bus CMOS EEPROM device. The DS28CZ04² 4kb I²C/SMBus™ EEPROM meets the SFP requirements. Its general-purpose I/O ports provide additional functionality to control a MAX3982 copper cable preemphasis driver or to report the state of the incoming signal at a MAX3748A receiver through the serial interface.

Circuit

Figure 1 shows the simplified schematic of the circuit used at either end of the cable. The box at the top left section represents the SFP connector with all signals and pin assignment. A cross reference between pin name and signal function is found in **Table 1**. The DS28CZ04 I²C memory chip connects to MOD-DEF1, MOD-DEF2, and transmitter power/ground. To reside on the correct SFP slave address, the address pins A1 and A2 need to be tied to ground. Write protect (WP) and master reset (MRZ) are not used; these pins are tied to ground (WP) and power (MRZ), respectively. PIO2 and PIO3 control the preemphasis inputs of U2, the MAX3982³ driver chip. The transmit data is routed AC-coupled from the SFP connector to the differential inputs of U2. The differential outputs directly drive the cable. The amplitude of the differential output can be set to one of two levels through the OUTLEV input, which is controlled by PIO1. For further information on how the remaining pins of U2 are connected, see the HFRD-16.0 document cited above.

In the schematic the output of the MAX3982 driver chip is controlled through the TX Disable signal coming from the SFP connector. This is one way to prevent activity at the differential output in case there is no data to be transmitted. Alternatively, one can ignore the external TX Disable signal and instead have the MAX3982 disable its output if it cannot detect data at its differential inputs. In this case, one connects the LOS output of the MAX3982 directly to the TX_DISABLE input of the MAX3982. The TX_DISABLE of the MAX3982 has an internal pull-up resistor. A third method combines automatic with controlled TX_DISABLE. This approach requires an additional 2 input OR gate with one of the inputs tied to TX Disable at the SFP connector and the other tied to the MAX3982 LOS output, which requires a 10kΩ pull-up resistor to VCCT. The output of the OR gate then drives the TX_DISABLE input of the MAX3982.

The incoming signal from the cable feeds AC-coupled into U3, the MAX3748A⁴ receiver, where it is restored to its

nominal amplitude. The restored signal is then routed AC-coupled to the SFP connector. If the signal from the cable is missing or the amplitude is too low, U3 asserts a LOS signal, which is routed to the SFP connector and to PIO0 of the DS28CZ04. The MAX3748A LOS output is an open collector, which requires a 4.7kΩ to 10kΩ pull-up resistor to VCCR in the host, as specified by the MSA. See the HDRD-16.0 document for details on how the remaining pins of U3 are connected.

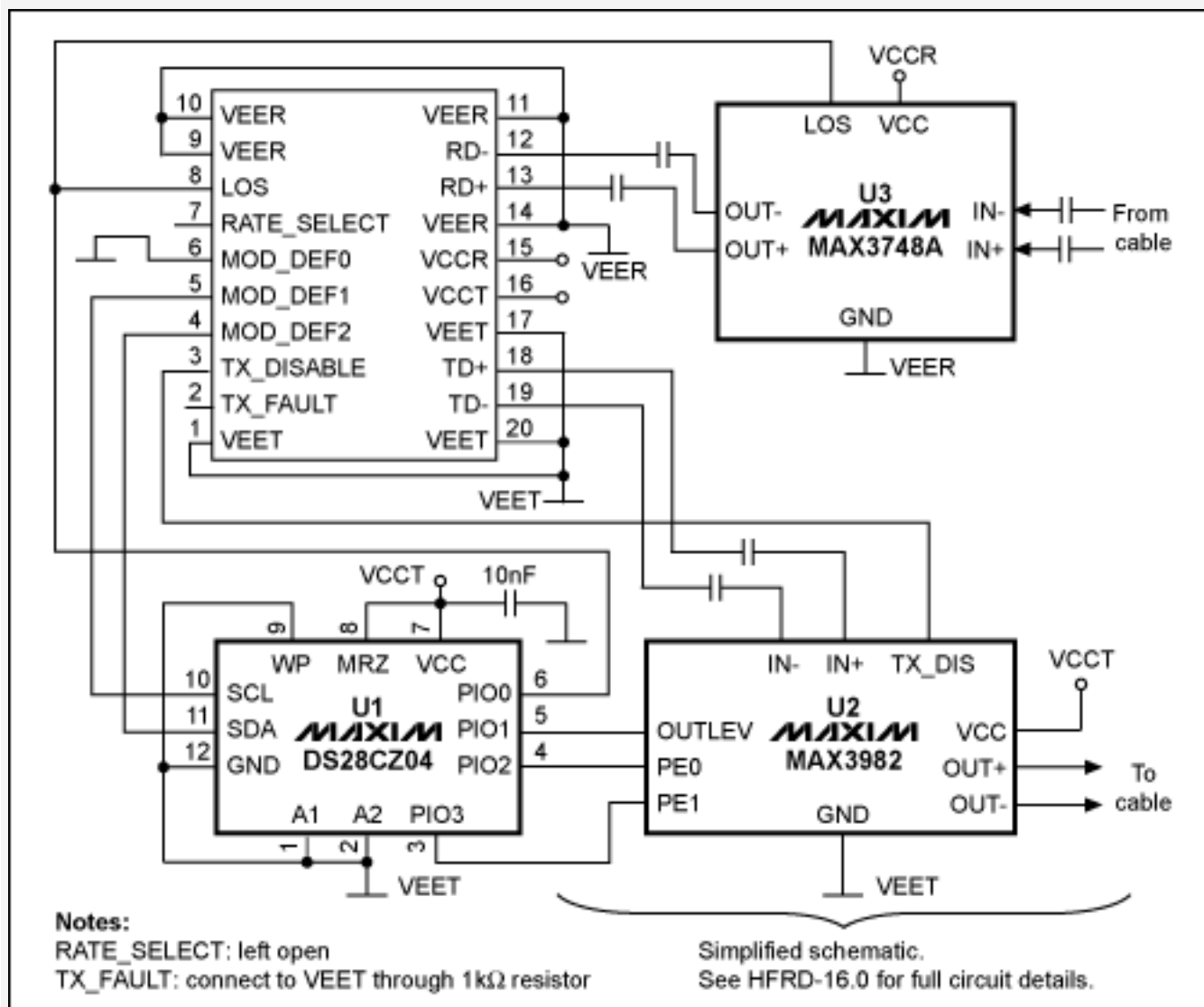


Figure 1. Simplified schematic of the DS28CZ04 in an active copper SFP cable assembly.

Table 1. SFP Connector Pin Assignment

Pin Number	Name	Function
1	VEET	Transmitter Ground
2	TX_FAULT	Transmitter Fault Indication, active-high; low indicates normal operation
3	TX_DISABLE	Transmitter Disable, active-high; low indicates normal operation
4	MOD_DEF2	Module Definition 2, SDA, I ² C data line
5	MOD_DEF1	Module Definition 1, SCL, I ² C clock line
6	MOD_DEFO	Module Definition 0, tied to ground on the board
7	RATE_SELECT	Optional Input: select between full or reduced receiver bandwidth; low/open indicates reduced bandwidth, high indicates full bandwidth
8	LOS	Loss of Signal (from receiver chip), active-high; low indicates normal operation
9	VEER	Receiver Ground
10	VEER	Receiver Ground
11	VEER	Receiver Ground
12	RD-	Inverted Received Data Out (from receiver chip)
13	RD+	Received Data Out (from receiver chip)
14	VEER	Receiver Ground
15	VCCR	Receiver Power, 3.3V \pm 5% DC
16	VCCT	Transmitter Power, 3.3V \pm 5% DC
17	VEET	Transmitter Ground
18	TD+	Transmit Data In (to transmitter chip)
19	TD-	Inverted Transmit Data In (to transmitter chip)
20	VEET	Transmitter Ground

DS28CZ04 as SFP Serial-Control Interface

The DS28CZ04 consists of a serial 2-wire interface, 4kb of EEPROM, and four bidirectional PIO channels, as shown in the block diagram in **Figure 2**. The device communicates with a host processor through its I²C interface in standard-mode or in fast-mode. The DS28CZ04 uses a single memory address byte and occupies two slave addresses, commonly referred to as Device Address A0h and A2h, to access all 512 memory locations.

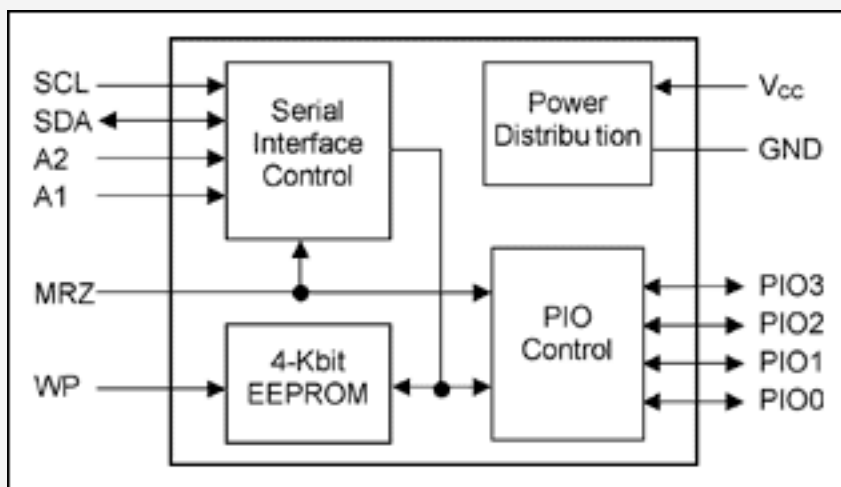


Figure 2. Block diagram of the DS28CZ04.

The DS28CZ04 has a memory range of 512 bytes, organized as two segments (lower half, upper half) of 256 bytes (**Tables 2A** and **2B**). The memory map and device addressing is compatible to SFF-8472 Digital

Diagnostic address assignments. The entire EEPROM can be write-protected by tying the WP pin to VCC. The PIO pins can be accessed through one address (i.e., single-address mode) or through separate addresses (i.e., multiaddress mode). PIO direct access addressing allows fast generation of data patterns and fast sampling.

The DS28CZ04 includes several EEPROM registers for the user to select whether the device powers up in SFF mode and to define the power-on default conditions for:

- Individual PIO output state (high, low, in output mode),
- Individual PIO data direction (in, out),
- Individual PIO output type (push-pull, open drain), and
- Individual PIO read bit inversion (true, false). Once powered up, the PIO settings can be overwritten through SRAM registers without affecting the power-on defaults.

Figure 3 shows a simplified schematic of a PIO. The flip-flops are accessed through the PIO R/W Access Registers and memory addresses 7Ah and 7Bh (device address = A0h). They are initialized at power-up or during reset according to the data stored at memory addresses 76h and 77h (device address = A0h). When a PIO is configured as input, the PIO output is tri-stated (high impedance). When a PIO is configured as output, the PIO input is the same as the output state XOR'ed with the corresponding read inversion bit.

Table 2A. Memory Map (Device Address = A0h)

Address	Type	Access	Description
00h to 74h	EEPROM	R/W	User memory
75h	EEPROM	R/W	Special function/user memory; controls whether device powers-up into SFF Mode
76h	EEPROM	R/W	Power-on default for PIO output state and direction for all PIOs
77h	EEPROM	R/W	Power-on default for PIO output type and read-inversion for all PIOs
78h to 79h	---	R	Reserved (reads FFh)
7Ah	SRAM	R/W	Actual direction setting for all PIOs and device control/status register
7Bh	SRAM	R/W	Actual PIO read-inversion and PIO output type for all PIOs
7Ch to 7Fh	SRAM	R/W	PIO read/write access registers
80h to FFh	EEPROM	R/W	User memory

Table 2B. Memory Map (Device Address = A2h)

ADDRESS	TYPE	ACCESS	DESCRIPTION
00h to 6Dh	EEPROM	R/W	User memory
6Eh	EEPROM	R/W	SFF mode off: user memory
	---	R	SFF mode on: SFF optional status Register
6Fh to EFh	EEPROM	R/W	User memory
F0h to FFh	---	R	Reserved (reads FFh)

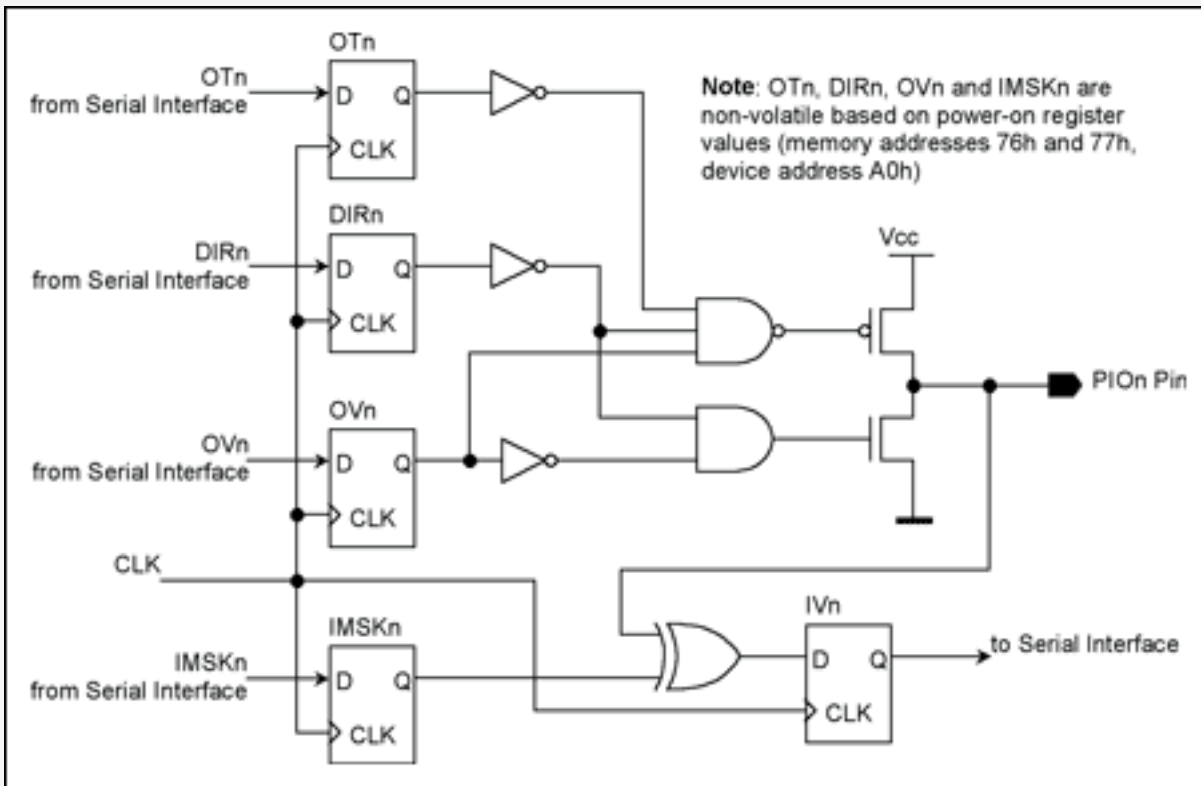


Figure 3. PIO simplified schematic.

Programming the DS28CZ04

The DS28CZ04 combines various control functions and the SFP identification and feature description in one convenient package. The advantage of the DS28CZ04 is its programmability, which allows different length cables to be used without needing to change components (e.g., straps or 0Ω resistors) on the board. Apart from the cable, the bill of material for the boards remains unchanged for an entire family of copper cable assemblies. For proper circuit function the memory of the DS28CZ04 must be programmed with the appropriate data as specified in the SFP MSA document or, alternatively, according to the Enhanced Digital Diagnostic Interface Definition of the **SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Xcvrs**.⁵

Special attention is required for the power-up default values that define the behavior of the four PIOs. For this application, PIO0 is an input and PIO1 to PIO3 are outputs. All outputs are defined as open drain, since the PE0, PE1 and OUTLEV inputs of the MAX3982 have internal pull-up resistors. Unless desired otherwise, PIO1, PIO2, and PIO3 shall power-up in high state, which is equivalent to maximum preemphasis and output signal as needed for a 15 to 20 meter cable. Input data from PIOs is read without inversion; using the SFF mode is optional. If selected, the LOS signal from the MAX3748A can be read as real-time diagnostics through memory address 6E (slave address A2h) of the DS28CZ04. SFF does not prohibit PIO0 and PIO1 functioning as outputs.

This power-up definition translates into the following data to be programmed into the power-on default registers. The **Tables 3** and **4** use the following color codes to explain the choice.

	Value resulting from configuration/application requirements
	Arbitrary assignment, "don't care" condition

Table 3. Power-On Default for PIO Output State (Lower Nibble) and Direction (Upper Nibble)

ADDR	b7	b6	b5	b4	b3	b3	b1	b0	Hex
76h	0	0	0	1	1	1	1	1	1F

Table 4. Power-On Default for PIO Read Inversion (Lower Nibble) and Output Type (Upper Nibble)

ADDR	b7	b6	b5	b4	b3	b3	b1	b0	Hex
76h	1	1	1	1	0	0	0	0	F0

The DS28CZ04 evaluation (EV) kit uses a PC. For more information on this EV kit, go to [DS28CZ04EVKIT](http://www.maxim-ic.com/DS28CZ04EVKIT) or please contact the factory for details.

Conclusion

The DS28CZ04 is a cost-efficient and very flexible serial-control interface chip for active copper SFP cable assemblies. It not only is compatible with SFP/MSA, but also with the **SFF-8472 Diagnostic Monitoring Interface for Optical Xcvrs**.

References

1. Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA) at: <http://www.schelto.com/SFP/SFP%20MSA.pdf>
2. [DS28CZ04 data sheet](#)
3. [MAX3982 data sheet](#)
4. [MAX3748A data sheet](#)
5. SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Xcvrs at: <ftp://ftp.seagate.com/sff/SFF-8472.PDF>

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AN3890, AN 3890, APP3890, Appnote3890, Appnote 3890

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