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APPLICATION NOTE 3838

Calculating Maximum Operating Frequency for Delay Lines

Abstract: Delay lines are used in applications that require a signal delay of a few nanoseconds (ns) or where incremental timing corrections are needed for the system to work properly. This application note discusses the maximum frequency that the input signal could have, and the maximum delay that can be obtained.

A similar version of this article was published on February 24, 2009 on the Industrial Control DesignLine website.

Calculating Maximum Input Frequency

When calculating the maximum input frequency, the critical parameter to consider is the minimum pulse width of the input signal. For periodic signals with a 50% duty cycle, the minimum pulse width would be half the period of the signal. This value, in turn, determines the maximum possible delay. Sometimes the input is periodic with a low frequency, but with a duty cycle of less than 50%. In this case, the width of the minimum duration between transitions (t_{WI}) on the input determines the minimum pulse width (**Figure 1**). In a number of devices, the minimum-input pulse width possible is specified as 100% of the maximum output delay desired (if not explicitly specified). The maximum output delay for these devices is, therefore (conversely), the same as the minimum-input pulse width.

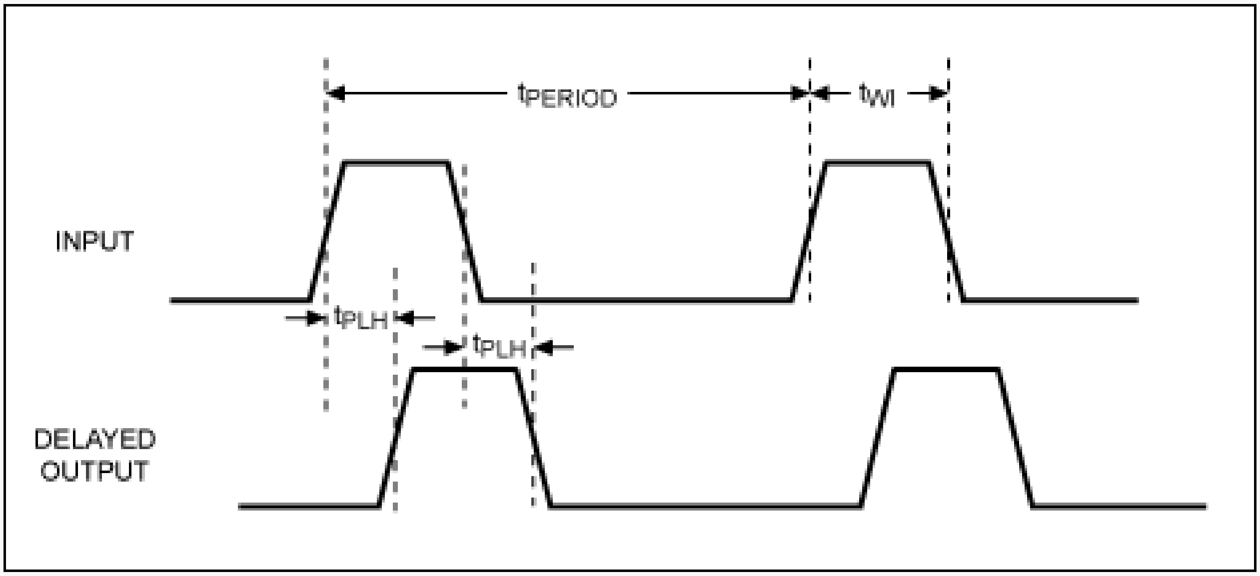

Figure 1. Illustration shows how the minimum duration between transitions (t_{WI}) of the input signal determines the maximum possible delay.

Maximum Input Frequency for Programmable Delay Lines

The specifications to consider for programmable delay lines are found in the product data sheet:

1. Zero-step delay (t_{PHL_MIN} or t_{PLH_MIN})

2. Minimum-input pulse width (t_{WI_MIN})

The minimum-input pulse width is usually specified explicitly in the data sheet, but is sometimes specified relative to the output delay desired. Therefore, to calculate the minimum-input pulse width, we consider the minimum delay that can be programmed, which is the same as the zero-step delay. The data sheet also specifies an error or tolerance over temperature and voltage. This error is added to the zero-step delay to determine the maximum zero-step delay. The maximum zero-step delay is essentially the minimum pulse width to consider (t_{WI_MIN}). The maximum frequency (f_{IN_MAX}) can then be calculated from the minimum-input pulse width using the following formula:

$$f_{IN\_MAX} = \frac{1}{2 \times t_{WI\_MIN}} \qquad \text{(Eq. 1)}$$

Table 1 gives some examples of the maximum allowable frequency for various devices.

Table 1. Maximum Input Frequencies for Programmable Delay Lines

Part Number	Description	Minimum or Zero-Step Delay, t_{PHL_MIN} or t_{PLH_MIN} (ns)	Maximum Zero-Step Delay (ns)	Minimum Pulse Width t_{WI_MIN} (ns)		Maximum Input Frequency (MHz)
DS1020-100	8-bit silicon delay line	10 ± 2	12	100% of output delay	12	41.67
DS1020-25	8-bit silicon delay line	10 ± 2	12	100% of output delay	12	41.67
DS1021-25	8-bit silicon delay line	10 ± 2	12	100% of output delay	12	41.67
DS1023-25	8-bit timing element	16.5	22	20	20	25
DS1023-500	8-bit timing element	16.5	22	50	50	10
DS1045-3	4-bit dual delay line	9 ± 1	10	100% of output delay	10	50

Maximum Input Frequency for Nonprogrammable Delay Lines

For nonprogrammable delay lines, the specifications to consider are also found in the product data sheet:

1. Delay at maximum tap position
2. Minimum-input pulse width (t_{WI_MIN})

The minimum-input pulse width is specified relative to the delay at maximum tap position. If an error is specified, it is added to this delay to obtain the maximum delay at the maximum tap position. This value is then used to calculate the minimum pulse width (t_{WI_MIN}). The maximum frequency (f_{IN_MAX}) can then be calculated from the minimum-input pulse width using Equation 1 above.

Table 2 shows some examples of the maximum allowable frequency for various nonprogrammable devices.

Table 2. Maximum Input Frequencies for Nonprogrammable Delay Lines

Part Number	Description	Delay at Maximum Tap Position	Maximum Delay at Max Tap Position	Minimum Pulse Width, t_{WI_MIN} (ns)		Maximum Input Frequency (MHz)
DS1110LE-200	3V, 10-tap silicon delay line	200	200	10% of tap 10 delay	20	25
DS1110LE-500	3V, 10-tap silicon delay line	500	500	10% of tap 10 delay	50	10
DS1135-6	3-in-1 high-speed silicon delay line	6 ± 1	7	100% of tap delay	7	71.43
DS1135-30	3-in-1 high-speed silicon delay line	30 ± 1.5	31.5	100% of tap delay	31.5	15.87

Calculating Maximum Frequency for an Application

For *programmable delay lines*: if a delay higher than the minimum delay is required, then the minimum pulse width allowable is calculated as:

Minimum Pulse Width = Maximum Step-Zero Delay + Programmed Delay.

The maximum allowable frequency can then be calculated using Equation 1.

Example for Programmable Delay Lines

1. Device used: DS1020-100
   Desired delay: 25ns
   Minimum pulse width = 25ns + 12ns = 37ns
   Maximum allowable input frequency = 1/(2 × 37ns) = 18.52MHz
2. Device used: DS1023-500
   Desired delay: 60ns
   Minimum pulse width = 22ns + 60ns = 82ns
   Maximum allowable input frequency = 1/(2 × 82ns) = 6.1MHz

For *non-programmable delay lines*: the minimum pulse width is independent of the delay tap used and, hence, remains the same as in Table 2.

Related Parts

DS1020: QuickView -- Full (PDF) Data Sheet

DS1020: QuickView -- Full (PDF) Data Sheet

DS1020: QuickView -- Full (PDF) Data Sheet

DS1021: QuickView -- Full (PDF) Data Sheet

DS1021: QuickView -- Full (PDF) Data Sheet

DS1021: QuickView -- Full (PDF) Data Sheet

DS1023: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS1023: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS1023: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS1045: QuickView -- Full (PDF) Data Sheet

DS1045: QuickView -- Full (PDF) Data Sheet

DS1045: QuickView -- Full (PDF) Data Sheet

DS1110: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS1110: QuickView -- Full (PDF) Data Sheet -- Free Samples

DS1110: QuickView -- Full (PDF) Data Sheet -- Free Samples

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