

Keywords: NVSRAM, PowerCap, SPM, Stik

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APPLICATION NOTE 3759

# Timing Considerations When Using NVSRAM

**Abstract:** This article assists in preparing the system memory timing for use with Maxim's nonvolatile SRAM (NVSRAM). Refer to the product data sheets for the referenced timing diagrams and minimum allowable delay values for each relevant parameter.

Maxim's NVSRAM modules are constructed using a Maxim nonvolatile controller, a low-power CMOS static RAM memory component, and a lithium coin-cell battery. Under normal operating conditions, read or write operations are functionally identical to a stand-alone SRAM. Using the parallel I/O structure, a user can easily store data to, or fetch data from any memory location defined by the address bus width. Subsequent memory cycles can occur at this, or any other location in any order desired with no duty cycle or write cycle-count restrictions.

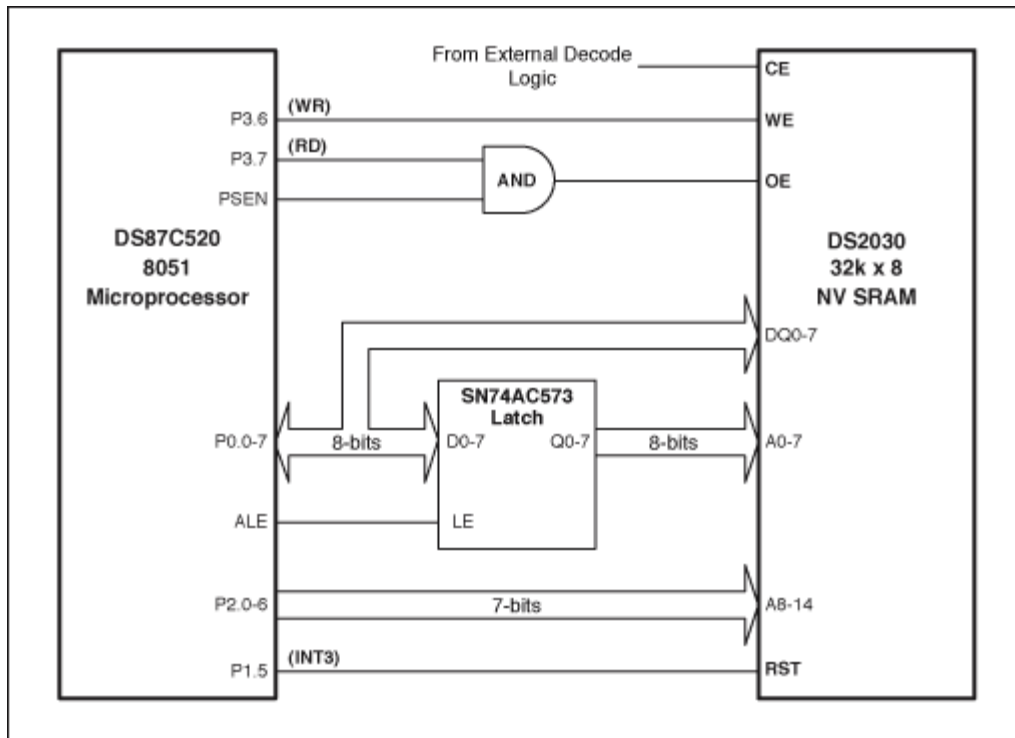


Figure 1. Typical NVSRAM circuit.

If the system power is above the specified write-protect voltage ( $V_{TP}$ ), the three control input pins (active-low CE, active-low WE, and active-low OE) define the memory operation to be performed, as depicted in Table 1. Write commands have priority over read commands. Maximum current consumption ( $I_{CC}$ ) for each state is specified in the DC Electrical Characteristics table in the product's data sheet.

Table 1. Operational Truth Table

$V_{CC}$	Active-Low CE	Active-Low WE	Active-Low OE	Address Bus	DQ Bus	Function	$I_{CC}$
$< V_{TP}$	x	x	x	x	High impedance	Write-protect	n/a
$> V_{TP}$	1	x	x	x	High impedance	Standby	$I_{CCS1}$ or $I_{CCS2}$
	0	1	1	Stable	High impedance	Read	$I_{CCO1}$
	0	1	0	Stable	Output data	Read	$I_{CCO1}$
	0	0	x	Stable	Input data	Write	$I_{CCO1}$

x = Do not care

$I_{CCS1}$  or  $I_{CCS2}$  is dependent upon the input voltage levels ( $V_{IH}/V_{IL}$ ) used.

## Suggested Rules for Robust Functional Operation

Three primary rules must always apply to any valid memory operation:

1.  $V_{CC}$  must be greater than the specified write-protect voltage ( $V_{TP}$ ) throughout the active memory cycle.
2. The address bus must be stable throughout the active memory cycle.
3. Cycle time of the active memory cycle ( $t_{RC}$  or  $t_{WC}$ ) should meet or exceed the minimum specified times listed in the data sheet.

## Understand the Timing Diagrams

It is important to remember that data-sheet timing diagrams generally show only one data line or address line in the depiction. In reality, you are providing at least eight data lines and over a dozen address lines probably with different signal-path lengths on the system board, and potentially with different loading characteristics on each signal. With a purely static memory, the last address and/or data signal to arrive at the device's input pins are the only ones that really count. The first address and/or data signal to change at the end of this memory operation are, again, the only ones that really count. Consequently, to avoid a classic timing race, take a few simple precautions in the timing definitions.

When defining system memory timing, it is also important to remember that an SRAM acts similar to a 'latch with depth.' You have to present your inputs (address and data) before you enable the controlling clock signal. This is defined as "setup time." You must also maintain that input condition (address and data) until the 'latch' operation completes. This is defined as "hold time." Hold times can vary according to which clock input is selected as the controlling signal.

## Write Cycles

As illustrated in Table 1, a **valid write** exists when ((active-low CE = 0) AND (active-low WE = 0)).

For a successful write operation to occur, the following conditions must be met:

1. The device must be enabled at the selected address for a minimum time (*Write Cycle*).
2. The write function must be enabled for a minimum time (*Write Pulse Width*).
3. The I/O pins (DQ0 through DQ7<sup>1</sup>) must be driven to a valid condition prior to (*Data Setup*), and held stable for some time after (*Data Hold*) the end point.

A write cycle starts when **valid write** becomes TRUE. It is performed at the address presented on the address pins. The start point is defined as the later occurring falling edge of either active-low CE<sup>2</sup> or active-low WE<sup>3</sup>.

A write cycle ends when **valid write** becomes FALSE. The end point is defined as the earlier occurring rising edge of either active-low CE<sup>2</sup> or active-low WE<sup>3</sup>.

Remembering Condition #2, no address changes are allowed during a **valid write**. Address timing must meet the *Address Setup* time requirements relative to the start point, the later falling edge of either active-low CE or active-low WE. All address lines must remain stable minimally until the end point.

With NVSRAM, there is an internal propagation delay exclusively through the active-low CE path. If using active-low WE to define the start and/or end points, follow the minimum timing requirements in the data sheet for the Write Cycle 1 illustration. If using active-low CE to define the start and/or end points, follow the minimum timing requirements in the data sheet for the Write Cycle 2 illustration.

Also remember that digital signals do not jump instantaneously from a logic 0 to a logic 1, as sometimes depicted in timing diagrams. Input-signal transition times can be difficult to predict at the system design stage, as that load characteristic is heavily dependant upon PC-board component placement, routing, and materials. To enhance the operational noise immunity in the final application, it is suggested that system setup and hold time delays exceed the data sheet minimums.

## Read Cycles

As illustrated in Table 1, a **valid read** exists when ((active-low CE = 0) AND (active-low WE = 1)), but no data out will appear

unless active-low OE = 0.

For a successful read operation to occur, these conditions must be met:

1. The device must be enabled at the selected address for a minimum time (*Read Cycle*).
2. The write function must be disabled.
3. The I/O pins (DQ0 through DQ7<sup>1</sup>) must be gated on for a minimum time (*active-low OE to Output Valid*) at or after the expected read access time (*active-low CE to Output Valid*).

A read cycle starts when **valid read** becomes TRUE. It is performed at the address presented on the address pins. The I/O pins become low impedance if active-low OE is also low<sup>4</sup>.

A read cycle ends when **valid read** becomes FALSE. The I/O pins become high impedance if active-low OE is also low<sup>4</sup>.

During a **valid read**, any address change that occurs after the expected read access time (*active-low CE to Output Valid*) terminates this memory cycle (Condition #2). When the address lines are again stable, the new address presented will trigger the beginning of a 'new' read cycle. The data from the first address is held valid at the I/O pins for some time after the address changed (*Output Hold*). The data from the 'new' address will be presented at the I/O pins by the address-activated access time (*Access Time*) from the point at which the last address input became stable.

During a **valid read**, any address change that occurs prior to the expected read access time (*active-low CE to Output Valid*) prematurely terminates this memory cycle. When the address lines are again stable, the new address presented will trigger a 'new' read cycle. The data from the first address are not guaranteed to be presented at the I/O pins. The data from the 'new' address will be presented at the I/O pins by the address-activated access time (*Access Time*), from the point at which the last address input became stable.

The I/O pins will drive data only when ((**valid read**) AND (active-low OE = 0)). This may be important for power consumption, as reduced device duty cycles and delayed output gating can reduce the component's current consumption.

If you have questions/comments/suggestions about this application note, please send them to: [MixedSignal.Apps@maxim-ic.com](mailto:MixedSignal.Apps@maxim-ic.com).

Notes:

1. For the DS1258, this applies to DQ0 through DQ15. For the DS2227 this applies to DQ0 through DQ31.
2. For the DS1258, this applies to active-low CEL or active-low CEU. For the DS2227, this applies to 1- active-low CE through 4- active-low CE.
3. For the DS2227, this applies to 1- active-low WE through 4- active-low WE.
4. For the DS2227, this applies to 1- active-low OE through 4- active-low OE.

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#### Related Parts

<a href="#">DS1220AB</a>	16k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1220AD</a>	16k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1225AB</a>	64k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1225AD</a>	64k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1230AB</a>	256k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1230W</a>	3.3V 256k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1230Y</a>	256k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1245AB</a>	1024k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1245W</a>	3.3V 1024k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1245Y</a>	1024k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1249AB</a>	2048k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1249W</a>	3.3V 2048kb Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1249Y</a>	2048k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1250AB</a>	4096k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1250W</a>	3.3V 4096k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1250Y</a>	4096k Nonvolatile SRAM	-- <a href="#">Free samples</a>
<a href="#">DS1265AB</a>	8M Nonvolatile SRAM	-- <a href="#">Free samples</a>

DS1265W	3.3V 8Mb Nonvolatile SRAM	-- Free samples
DS1265Y	8M Nonvolatile SRAM	-- Free samples
DS1270AB	16M Nonvolatile SRAM	-- Free samples
DS1270W	3.3V 16Mb Nonvolatile SRAM	-- Free samples
DS1270Y	16M Nonvolatile SRAM	-- Free samples
DS1330AB	256k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1330W	3.3V 256k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1330Y	256k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1345AB	1024k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1345W	3.3V 1024k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1345Y	1024k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1350AB	4096k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1350W	3.3V 4096K Nonvolatile SRAM with Battery Monitor	-- Free samples
DS1350Y	4096k Nonvolatile SRAM with Battery Monitor	-- Free samples
DS2227	Flexible NV SRAM Stik	

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