

APPLICATION NOTE 3686

DS2155 and DS26521 Software Comparison

This application note describes the differences between the DS2155 and DS26521 single-port devices. They each contain a framer and LIU combination for T1, E1, and J1 applications and support both long-haul and short-haul lines. This note contains a complete breakdown of all feature differences and compares the two devices on a register-by-register basis.

Indirect Registers

The DS2155 uses indirect registers for the following 1per-channel functions. The DS26521 uses direct registers for these functions. The DS26521 only uses indirect registers for loading repetitive patterns, up to 512 bytes, in the BERT.

DS2155 Indirect Register Function	DS26521 Direct Register	Comments
Per-channel transmit idle code	TIDR1 to TIDR32	
Per-channel receive idle code	RIDR1 to RIDR24	
BERT transmit channel select	TBCS1 to TBCS4	
Transmit fractional channel select	TGCCS1 to TGCCS4	
Payload error insert channel select	–	Not supported
Transmit hardware signaling channel select	SSIE1 to SSIE4	
BERT receive channel select	RBCS1 to RBCS4	
Receive fractional channel select	RGCCS1 to RGCCS4	
Receive signaling reinsertion channel select	RSI1 to RSI4	
Receive signaling all-ones insertion channel select	T1RSAOI1 to T1RSAOI3	T1 mode

Terminology

Some of the terminology used in the DS26521 data sheet is different from previous T1/E1 data sheets from Dallas Semiconductor. For example, previous data sheets used the acronym RLOS to refer to Receive Loss of Sync. In the DS26521 data sheet, RLOS more correctly refers to Receive Loss of Signal. The table below shows the differences.

Condition	DS26521 Data Sheet	Previous Data Sheets
Loss of in-bound signal	RLOS (Receive Loss Of Signal)	RCL (Receive Carrier Loss)
Loss of synchronization	RLOF (Receive Loss OF Framing)	RLOS (Reive Loss Of Synchronization)
In-bound all ones	AIS (Alarm Indication Signal) T1 and E1 modes	AIS for E1 mode blue alarm for T1 mode
Remote alarm	RAI (Remote Alarm Indication) T1 and E1 modes	RAI for E1 mode yellow alarm for T1 mode

Register Mapping

The DS26521 address map is compatible with the Maxim/Dallas Semiconductor octal framer products, DS26401, the DS26524 Quad SCT, and the DS26528 Octal SCT. (All addresses are shown in hexadecimal in this application note.) The table below shows the register control functions of the framer, LIU, and BERT in the DS26521.

Register Address Ranges (in Hex)

Address Range	Block
0000 – 00EF	Receive framer
00F0 – 00FF	Global registers
0100 – 01EF	Transmit framer
1000 – 1017	LIU
1018 – 101F	Test
1100 – 110F	BERT

Direct Register Mapping

The following registers in the DS2155 can be mapped directly to registers in the DS26521.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Address	DS26521 Symbol
08	SSIE1	Software signaling insertion enable 1	118	SSIE1
09	SSIE2	Software signaling insertion enable 2	119	SSIE2
0A	SSIE3	Software signaling insertion enable 3	120	SSIE3
0B	SSIE4	Software signaling insertion enable 4	121	SSIE4
0C	T1RDMR1	T1 receive digital milliwatt enable register 1	03C	T1RDMWE1
0D	T1RDMR2	T1 receive digital milliwatt enable register 2	03D	T1RDMWE2
0E	T1RDMR3	T1 receive digital milliwatt enable register 3	03E	T1RDMWE3
0F	IDR	Device identification register	0F8	IDR
38	RSINFO1	Receive signaling change-of-state information 1	098	RSS1
39	RSINFO2	Receive signaling change-of-state information 2	099	RSS2
3A	RSINFO3	Receive signaling change-of-state information 3	09A	RSS3
3B	RSINFO4	Receive signaling change-of-state information 4	09B	RSS4
3C	RSCSE1	Receive signaling change-of-state interrupt enable 1	0A8	RSCSE1
3D	RSCSE2	Receive signaling change-of-state interrupt enable 2	0A9	RSCSE2
3E	RSCSE3	Receive signaling change-of-state interrupt enable 3	0AA	RSCSE3
3F	RSCSE4	Receive signaling change of-state interrupt enable 4	0AB	RSCSE4
42	LCVCR1	Line code violation count register 1	050	LCVCR1
43	LCVCR2	Line code violation count register 2	051	LCVCR2
44	PCVCR1	Path code violation count register 1	052	PCVCR1
45	PCVCR2	Path code violation count register 2	053	PCVCR2
46	FOSCR1	Frames out-of-sync count register 1	054	FOSCR1
47	FOSCR2	Frames out-of-sync count register 2	055	FOSCR2
48	EBCR1	E-bit count register 1	056	E1EBCR1
49	EBCR2	E-bit count register 2	057	E1EBCR2
4B	PCLR1	Per-channel loopback enable register 1	1D0	PCL1
4C	PCLR2	Per-Channel loopback enable register 2	1D1	PCL2
4D	PCLR3	Per-Channel loopback enable register 3	1D2	PCL3
4E	PCLR4	Per-Channel loopback enable register 4	1D3	PCL4
50	TS1	Transmit signaling register 1	140	TS1
51	TS2	Transmit signaling register 2	141	TS2
52	TS3	Transmit signaling register 3	142	TS3
53	TS4	Transmit signaling register 4	143	TS4
54	TS5	Transmit signaling register 5	144	TS5
55	TS6	Transmit signaling register 6	145	TS6
56	TS7	Transmit signaling register 7	146	TS7
57	TS8	Transmit signaling register 8	147	TS8
58	TS9	Transmit signaling register 9	148	TS9
DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Address	DS26521 Symbol

59	TS10	Transmit signaling register 10	149	TS10
5A	TS11	Transmit signaling register 11	14A	TS11
5B	TS12	Transmit signaling register 12	14B	TS12
5C	TS13	Transmit signaling register 13	14C	TS13
5D	TS14	Transmit signaling register 14	14D	TS14
5E	TS15	Transmit signaling register 15	14E	TS15
5F	TS16	Transmit signaling register 16	14F	TS16
60	RS1	Receive signaling register 1	040	RS1
61	RS2	Receive signaling register 2	041	RS2
62	RS3	Receive signaling register 3	042	RS3
63	RS4	Receive signaling register 4	043	RS4
64	RS5	Receive signaling register 5	044	RS5
65	RS6	Receive signaling register 6	045	RS6
66	RS7	Receive signaling register 7	046	RS7
67	RS8	Receive signaling register 8	047	RS8
68	RS9	Receive signaling register 9	048	RS9
69	RS10	Receive signaling register 10	049	RS10
6A	RS11	Receive signaling register 11	04A	RS11
6B	RS12	Receive signaling register 12	04B	RS12
6C	RS13	Receive signaling register 13	04C	RS13
6D	RS14	Receive signaling register 14	04D	RS14
6E	RS15	Receive signaling register 15	04E	RS15
6F	RS16	Receive signaling register 16	04F	RS16
74	TDS0SEL	Transmit DS0 monitor select	189	TDS0SEL
75	TDS0M	Transmit DS0 monitor register	1BB	TDS0M
76	RDS0SEL	Receive DS0 monitor select	012	RDS0SEL
77	RDS0M	Receive DS0 monitor register	060	RDS0M
80	TCICE1	Transmit idle code enable register 1	150	TCICE1
81	TCICE2	Transmit idle code enable register 2	151	TCICE2
82	TCICE3	Transmit idle code enable register 3	152	TCICE3
83	TCICE4	Transmit idle code enable register 4	153	TCICE4
84	RCICE1	Receive idle code enable register 1	0D0	RCICE1
85	RCICE2	Receive idle code enable register 2	0D1	RCICE2
86	RCICE3	Receive idle code enable register 3	0D2	RCICE3
87	RCICE4	Receive idle code enable register 4	0D3	RCICE4
88	RCBR1	Receive channel blocking register 1	0C4	RCBR1
89	RCBR2	Receive channel blocking register 2	0C5	RCBR2
8A	RCBR3	Receive channel blocking register 3	0C6	RCBR3
8B	RCBR4	Receive channel blocking register 4	0C7	RCBR4
8C	TCBR1	Transmit channel blocking register 1	1C4	TCBR1
8D	TCBR2	Transmit channel blocking register 2	1C5	TCBR2
8E	TCBR3	Transmit channel blocking register 3	1C6	TCBR3
8F	TCBR4	Transmit channel blocking register 4	1C7	TCBR4
B7	TCD1	Transmit code definition register 1	1AC	T1TCD1
B8	TCD2	Transmit code definition register 2	1AD	T1TCD2
B9	RUPCD1	Receive up code definition register 1	0AC	T1RUPCD1
BA	RUPCD2	Receive up code definition register 2	0AD	T1RUPCD2
BB	RDNCD1	Receive down code definition register 1	0AE	T1RDNCD1
BC	RDNCD2	Receive down code definition register 2	0AF	T1RDNCD2
BE	RSCD1	Receive spare code definition register 1	09C	T1RSCD1
BF	RSCD2	Receive spare code definition register 2	09D	T1RSCD2
DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Address	DS26521 Symbol
C0	RFDL	Receive FDL register	062	T1RFDL
C1	TFDL	Transmit FDL register	162	T1TFDL

C6	RAF	Receive align frame register	064	E1RAF
C7	RNAF	Receive nonalign frame register	065	E1RNAF
C8	RSiAF	Receive Si align frame	066	E1RSiAF
C9	RSiNAF	Receive Si nonalign frame	067	E1RSiNAF
CA	RRA	Receive remote alarm bits	068	E1RRA
CB	RSa4	Receive Sa4 bits	069	E1RSa4
CC	RSa5	Receive Sa5 bits	06A	E1RSa5
CD	RSa6	Receive Sa6 bits	06B	E1RSa6
CE	RSa7	Receive Sa7 bits	06C	E1RSa7
CF	RSa8	Receive Sa8 bits	06D	E1RSa8
D0	TAF	Transmit align frame register	164	E1TAF
D1	TNAF	Transmit nonalign frame register	165	E1TNAF
D2	TSiAF	Transmit Si align frame	166	E1TSiAF
D3	TSiNAF	Transmit Si nonalign frame	167	E1TSiNAF
D4	TRA	Transmit remote alarm bits	168	E1TRA
D5	TSa4	Transmit Sa4 bits	169	E1TSa4
D6	TSa5	Transmit Sa5 bits	16A	E1TSa5
D7	TSa6	Transmit Sa6 bits	16B	E1TSa6
D8	TSa7	Transmit Sa7 bits	16C	E1TSa7
D9	TSa8	Transmit Sa8 bits	16D	E1TSa8
DA	TSACR	Transmit Sa bit control register	114	E1TSACR

Bit-Level Mapping

The following registers in the DS2155 do not have direct mapping to registers in the DS26521. The following table shows how to map the individual bits of the DS2155 registers into the individual bits of the DS26521 registers.

***Note:** **NS** = not supported

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
00	MSTRREG	Master mode register	0 = RMMR.1 & TMMR.1 1 = RMMR.0 & TMMR.0 2 = NS 3 = NS 4 = -- 5 = -- 6 = -- 7 = --	
01	IOCR1	I/O configuration register 1	0 = TCR3.7 1 = TIOCR.2 2 = TIOCR.0 3 = TIOCR.1 4 = RIOCR.2 5 = RIOCR.0 6 = RIOCR.1 7 = RIOCR.3	
02	IOCR2	I/O configuration register 2	0 = RIOCR.4 1 = TIOCR.4 2 = RIOCR.5 3 = TIOCR.5 4 = TIOCR.6 5 = RIOCR.6 6 = TIOCR.7 7 = RIOCR.7	
03	T1RCR1	T1 receive control register 1	0 = RCR1.0 1 = RCR1.1 2 = RCR1.7 3 = RCR1.3 4 = T1RCR2.2 5 = T1RCR2.3 6 = RCR1.4 7 = --	
04	T1RCR2	T1 receive control register 2	0 = T1RCR2.0 1 = RCR1.2 2 = NS * 3 = NS ** 4 = T1RCR2.4 5 = RCR1.6 6 = RCR1.5 7 = --	* ZBTSI not supported in the DS26521. ** Information available in HDLC section.
05	T1TCR1	T1 transmit control register 1	0 = TCR1.0 * 1 = TCR1.1 * 2 = TCR2.7 * 3 = TCR1.3 * 4 = TCR1.4 * 5 = TCR1.5 * 6 = TCR1.6 * 7 = TCR1.7 *	* T1 mode

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
06	T1TCR2	T1 transmit control register 2	0 = TCR2.0 *** 1 = NS * 2 = TCR2.2 *** 3 = TCR2.3 *** 4 = TCR2.4 *** 5 = NS ** 6 = TCR2.6 *** 7 = TCR1.2 ***	* ZBTSI not supported in the DS26521. ** Information available in HDLC section. *** T1 mode
07	T1CCR1	T1 common control register 1	0 = TCR3.0 1 = TCR2.1 * 2 = TCR3.2 3 = TCR4.2 * 4 = TCR4.3 * 5 = -- 6 = -- 7 = --	* T1 mode
10	INFO1	Information register 1	0 = RLS2.0 * 1 = RLS2.1 * 2 = RLS2.2 * 3 = RLS2.3 * 4 = RLS2.4 * 5 = RLS2.5 * 6 = TLS1.3 7 = RLS2.7 *	* T1 mode
11	INFO2	Information register 2	0 = NS 1 = NS 2 = NS 3 = NS 4 = LLSR.2 5 = NS 6 = RLS7.0 * 7 = NS **	* T1 mode ** Information available in BERT section.
12	INFO3	Information register 3	0 = RLS2.5 * 1 = RLS2.4 * 2 = RLS2.6 * 3 = -- 4 = -- 5 = -- 6 = -- 7 = --	* E1 mode
13		UNUSED		
14	IIR1	Interrupt information register 1		Consult RIIR and TIIR DS26521 registers.
15	IIR2	Interrupt information register 2		Consult RIIR and TIIR DS26521 registers.
16	SR1	Status register 1	0 = TLS1.0 & TLS1.1* 1 = LLSR.2 & LLSR.6 * 2 = NS 3 = LLSR.0 & LLSR.4 * 4 = LLSR.3 & LLSR.7 * 5 = RLS4.3 6 = RLS4.1 7 = NS	* The DS26521 uses separate interrupt detect and clear bits, while the DS2155 uses a double-pollled interrupt bit.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
17	IMR1	Interrupt mask register 1	0 = TIM1.0 & TIM1.1* 1 = LSIMR.2 & LSIMR.6* 2 = NS 3 = LSIMR.0 & LSIMR.4* 4 = LSIMR.3 & LSIMR.7* 5 = RIM4.3 6 = RIM4.1 7 = NS	* The DS26521 uses separate interrupt detect and clear bits, while the DS2155 uses a double-pollled interrupt bit.
18	SR2	Status register 2	0 = RLS1.0* 1 = RLS1.1** 2 = RLS1.2 3 = RLS1.3 4 = RLS1.4 5 = RLS1.5 6 = RLS1.6 7 = RLS1.7	* The DS2155 data sheet uses the acronym RLOS (Receive Loss Of Synchronization) to refer to RLOF (Receive Loss Of Frame). ** The DS2155 data sheet uses the acronym RCL (Receive Carrier Loss) to refer to RLOS (Receive Loss Of Signal).
19	IMR2	Interrupt mask register 2	0 = RIM1.0 1 = RIM1.1 2 = RIM1.2 3 = RIM1.3 4 = RIM1.4 5 = RIM1.5 6 = RIM1.6 7 = RIM1.7	
1A	SR3	Status register 3	0 = RLS1.3 & RLS1.6* 1 = RLS3.0 & RLS3.4** 2 = RLS3.1 & RLS3.5** 3 = RLS3.3 & RLS3.7 4 = TLS1.0 & TLS1.1* 5 = RLS3.0 & RLS3.4*** 6 = RLS3.1 & RLS3.5*** 7 = RLS3.2 & RLS3.6***	* The DS26521 uses separate interrupt detect and clear bits, while the DS2155 uses a double-pollled interrupt bit. ** E1 mode *** T1 mode
1B	IMR3	Interrupt mask register 3	0 = RIM1.3 & RIM1.7* 1 = RIM3.0 & RIM3.4** 2 = RIM3.1 & RIM3.5** 3 = RIM3.3 & RIM3.6** 4 = TIM1.0 & TIM1.1* 5 = RIM3.0 & RIM3.4*** 6 = RIM3.1 & RIM3.5*** 7 = RIM3.2 & RIM3.6***	* The DS26521 uses separate interrupt detect and clear bits, while the DS2155 uses a double-pollled interrupt bit. ** E1 mode *** T1 mode
1C	SR4	Status register 4	0 = RLS2.0* 1 = RLS2.1* 2 = RLS4.0 3 = TLS1.3* 4 = TLS1.2 5 = RLS2.2* 6 = RLS2.3* 7 = RLS7.4**	* E1 mode ** T1 mode

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
1D	IMR4	Interrupt mask register 4	0 = RIM2.0 * 1 = RIM2.1 * 2 = RIM4.0 3 = TIM1.3 * 4 = TIM1.2 5 = RIM2.2 * 6 = RIM2.3 * 7 = RIM7.4 **	* E1 mode ** T1 mode
1E	SR5	Status register 5	0 = RLS4.5 1 = RLS4.6 2 = RLS4.7 3 = TLS1.5 4 = TLS1.6 5 = TLS1.7 6 = -- 7 = --	
1F	IMR5	Interrupt mask register 5	0 = RIM4.5 1 = RIM4.6 2 = RIM4.7 3 = TIM1.5 4 = TIM1.6 5 = TIM1.7 6 = -- 7 = --	
20	SR6	Status register 6		Information available in HDLC section.
21	IMR6	Interrupt mask register 6		Information available in HDLC section.
22	SR7	Status register 7		Information available in HDLC section.
23	IMR7	Interrupt mask register 7		Information available in HDLC section.
24	SR8	Status register 8	0 = RLS7.0 * 1 = NS 2 = TLS2.4 3 = RLS7.2 * 4 = NS 5 = RLS7.1 * 6 = -- 7 = --	* T1 mode
25	IMR8	Interrupt mask register 8	0 = RIM7.0 * 1 = NS 2 = TIM2.4 3 = RIM7.2 * 4 = NS 5 = RIM7.1 * 6 = -- 7 = --	* T1 mode
26	SR9	Status register 9		Information available in BERT section.
27	IMR9	Interrupt mask register 9		Information available in BERT section.
28	PCPR	Per-channel pointer register		Information is in Indirect Register section.
29	PCDR1	Per-channel data register 1		Information is in Indirect Register section.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
2A	PCDR2	Per-channel data register 2		Information is in Indirect Register section.
2B	PCDR3	Per-channel data register 3		Information is in Indirect Register section.
2C	PCDR4	Per-channel data register 4		Information is in Indirect Register section.
2D	INFO4	Information register 4		Information available in HDLC section.
2E	INFO5	Information register 5		Information available in HDLC section.
2F	INFO6	Information register 6		Information available in HDLC section.
30	INFO7	Information register 7	0 = E1RRTS7.2 * 1 = E1RRTS7.1 * 2 = E1RRTS7.0 * 3 = E1RRTS7.3 * 4 = E1RRTS7.4 * 5 = E1RRTS7.5 * 6 = E1RRTS7.6 * 7 = E1RRTS7.7 *	* E1 mode
31	H1RC	HDLC #1 receive control		Information available in HDLC section.
32	H2RC	HDLC #2 receive control		Unsupported function in the DS26521.
33	E1RCR1	E1 receive control register 1	0 = RCR1.0 * 1 = RCR1.1 * 2 = RCR1.2 * 3 = RCR1.3 * 4 = RCR1.4 * 5 = RCR1.6 * 6 = RCR1.5 * 7 = RCR3.5	* E1 mode
34	E1RCR2	E1 receive control register 2	0 = E1RCR2.0 * 1 = -- 2 = -- 3 = E1RCR2.3 * 4 = E1RCR2.4 * 5 = E1RCR2.5 * 6 = E1RCR2.6 * 7 = E1RCR2.7 *	* E1 mode
35	E1TCR1	E1 transmit control register 1	0 = TCR1.0 * 1 = TCR1.5 * 2 = TCR1.2 * 3 = TCR1.3 * 4 = TCR1.4 * 5 = TCR1.1 * 6 = TCR1.6 * 7 = TCR1.7 *	* E1 mode
36	E1TCR2	E1 transmit control register 2	0 = TCR2.5 * 1 = TCR2.6 * 2 = TCR2.7 * 3 = TCR2.4 * 4 = TCR2.3 * 5 = TCR2.2 * 6 = TCR2.1 * 7 = TCR2.0 *	* E1 mode

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
37	BOCC	BOC control register	0 = THC2.6 1 = T1RBOCC.1 2 = T1RBOCC.2 3 = T1RBOCC.7 4 = NS * 5 = -- 6 = -- 7 = --	* The DS26521 has a dedicated receive BOC message register.
40	SIGCR	Signaling control register	0 = RSIGC.4 * 1 = NS 2 = NS 3 = RSIGC.2 4 = RSIGC.1 5 = -- 6 = -- 7 = NS **	* The DS26521 forces signaling to all ones on a per-channel basis using the T1RSAOI1 to T1RSAOI4 registers. ** The DS26521 selects signaling re-insertion on a per-channel basis using the RSI1 to RSI4 registers.
41	ERCNT	Error count configuration register	0 = ERCNT.0 1 = ERCNT.1 * 2 = ERCNT.2 * 3 = NS 4 = ERCNT.3 5 = ERCNT.4 6 = ERCNT.5 7 = --	* T1 mode only
4A	LBCR	Loopback control register	0 = RCR3.0 1 = RCR3.1 2 = LMCR.3 3 = LMCR.5 4 = NS 5 = -- 6 = -- 7 = --	
4F	ESCR	Elastic store control register	0 = RESCR.0 1 = RESCR.1 2 = RESCR.2 3 = RESCR.3 4 = TESCR.0 5 = TESCR.1 6 = TESCR.2 7 = TESCR.3	
70	CCR1	Common control register 1	0 = GTCR1.5 1 = TCR3.4 2 = TCR3.5 3 = NS * 4 = TCR3.6 5 = RSIGC.0 6 = TCR3.0 ** 7 = NS	* The DS26521 does not use indirect registers. ** E1 mode

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
71	CCR2	Common control register 2	0 = NS * 1 = GFCR.4 ** 2 = GFCR.5 ** 3 = -- 4 = -- 5 = -- 6 = -- 7 = --	* Backplane clock is always enabled. ** The setting is the opposite of the setting in the DS2155. See the DS26521 datasheet for detail.
72	CCR3	Common control register 3	0 = RESCR.6 1 = RESCR.7 2 = TESCR.6 3 = TESCR.7 4 = -- 5 = -- 6 = GTCR1.0 7 = NS *	* Unsupported function in the DS26521.
73	CCR4	Common control register 4	0 = NS * 1 = NS * 2 = NS * 3 = NS * 4 = NS 5 = NS 6 = NS 7 = NS	* The DS26521 does not have user-definable output pins.
78	LIC1	Line interface control 1	0 = LMCR.2 1 = NS 2 = LTRCR.4 3 = LTRCR.2 & LTRCR.3 4 = NS 5 = LTITSR.0 6 = LTITSR.1 7 = LTITSR.2	
79	LIC2	Line interface control 2	0 = NS 1 = NS 2 = -- 3 = NS 4 = TCR1.1 * 5 = TCR3.1 6 = NS ** 7 = LTRCR.1	* E1 mode ** The DS26521 has a global register (GLSRR) to reset each LIU. See the DS26521 datasheet for detail.
7A	LIC3	Line interface control 3	0 = NS 1 = NS 2 = LRISMR.7 3 = NS 4 = NS 5 = NS 6 = NS 7 = --	
7B	LIC4	Line interface control 4	0 = NS 1 = NS 2 = NS 3 = NS 4 = NS * 5 = * 6 = NS 7 = NS	* Consult GTCCR.0-1 register in the DS26528 datasheet.
7C		UNUSED		

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
7D	TLBC	Transmit line build-out control		Unsupported function in the DS26521.
7E	IAAR	Idle array address register		The DS26521 does not use direct registers.
7F	PCICR	Per-channel idle code value register		The DS26521 does not use direct registers.
90 - 9F	HDLC1	HDLC #1 functions registers		Information available in HDLC section.
A0 - AF	HDLC2	HDLC #2 functions registers		Unsupported function in the DS26521.
B0	ESIBCR1	Extend system information bus control register 1		Unsupported function in the DS26521.
B1	ESIBCR2	Extend system information bus control register 2		Unsupported function in the DS26521.
B2	ESIB1	Extend system information bus register 1		Unsupported function in the DS26521.
B3	ESIB2	Extend system information bus register 2		Unsupported function in the DS26521.
B4	ESIB3	Extend system information bus register 3		Unsupported function in the DS26521.
B5	ESIB4	Extend system information bus register 4		Unsupported function in the DS26521.
B6	IBCC	In-band code control register	0 = T1RIBCC.0 * 1 = T1RIBCC.1 * 2 = T1RIBCC.2 * 3 = T1RIBCC.3 * 4 = T1RIBCC.4 * 5 = T1RIBCC.5 * 6 = TCR4.0 * 7 = TCR4.1 *	* T1 mode only
BD	RSCC	In-band receive spare control register	0 = T1RSCC.0 1 = T1RSCC.1 2 = T1RSCC.2 3 = -- 4 = -- 5 = -- 6 = -- 7 = --	
C2	RFDLM1	Receive FDL match register 1		Unsupported function in the DS26521.
C3	RFDLM2	Receive FDL match register 2		Unsupported function in the DS26521.
C4		Unused		Unused

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
C5	IBOC	Interleave bus operation control register	0 = TIBOC.0 1 = TIBOC.1 2 = TIBOC.2 3 = TIBOC.3 4 = TIBOC.4 5 = TIBOC.5 6 = TIBOC.6 7 = --	
DB - E1	BERT	BERT functions registers		Information available in BERT section.
E2		Unused		Unused
E3 - EF	BERT	BERT functions registers		Information available in BERT section.
F0 - FF	TEST	Test register	Address 1018 – 101F	

HDLC Controller

The DS26521 has a single HDLC controller that can be mapped to any time slot or to the FDL (T1 mode), or to any combinations of Sa bits (E1 mode). The table below lists the differences between the DS2155's and the DS26521's HDLC function.

	DS2155	DS26521
Number of controllers	2	1
FIFO size	128 Bytes	64 Bytes
Channel assignment	Any combination of channels, facilities data link (FDL) bit stream, any combinations of Sa bits	Any single DS0, facilities data link (FDL) bit stream, any combination of Sa bits
SS7 support	Yes	No

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
31	H1RC	HDLC #1 receive control	0 = NS * 1 = -- 2 = -- 3 = -- 4 = -- 5 = -- 6 = RHC.5 7 = RHC.6	* The DS26521 does not have support for Signaling System 7 (SS7).
32	H2RC	HDLC #2 receive control		Unsupported function in the DS26521.
90	H1TC	HDLC #1 transmit control	0 = THC1.0 1 = THC1.1 2 = THC1.2 3 = THC1.3 4 = THC1.4 5 = THC1.5 6 = THC1.6 7 = THC1.7	
91	H1FC	HDLC #1 FIFO control	0 = RHFC.0 1 = RHFC.1 2 = NS * 3 = THFC.0 4 = THFC.1 5 = NS * 6 = -- 7 = --	* The HDLC FIFO is only 64 bytes deep on the DS26521.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
92	H1RCS1	HDLC #1 receive channel select 1		The DS26521 uses the RHC register to select the channel to receive HDLC data. The DS26521 can only receive HDLC data in a single DSO channel.
93	H1RCS2	HDLC #1 receive channel select 2		
94	H1RCS3	HDLC #1 receive channel select 3		
95	H1RCS4	HDLC #1 receive channel select 4		
96	H1RTSBS	HDLC #1 receive Time Slot Bits/Sa Bits select	NS	
97	H1TCS1	HDLC #1 transmit channel select 1		The DS26521 uses the THC2 register to select the channel to transmit HDLC data. The DS26521 can only transmit HDLC data in a single DSO channel.
98	H1TCS2	HDLC #1 transmit channel select 2		
99	H1TCS3	HDLC #1 transmit channel select 3		
9A	H1TCS4	HDLC #1 transmit channel select 4		
9B	H1TTSBS	HDLC #1 transmit time- slot bits/Sa bits select	NS	
9C	H1RPBA	HDLC #1 receive packet bytes available	0B5 RHPBA	
9D	H1TF	HDLC #1 transmit FIFO	1B4 THF	
9E	H1RF	HDLC #1 receive FIFO	0B6 RHF	
9F	H1TFBA	HDLC #1 transmit FIFO buffer available	1B3 TFBA	
A0	H2TC	HDLC #2 transmit control		Unsupported function in the DS26521.
A1	H2FC	HDLC #2 FIFO control		Unsupported function in the DS26521.
A2	H2RCS1	HDLC #2 receive channel select 1		Unsupported function in the DS26521.
A3	H2RCS2	HDLC #2 receive channel select 2		Unsupported function in the DS26521.
A4	H2RCS3	HDLC #2 receive channel select 3		Unsupported function in the DS26521.
A5	H2RCS4	HDLC #2 receive channel select 4		Unsupported function in the DS26521.
A6	H2RTSBS	HDLC #2 receive time-slot bits/Sa bits select		Unsupported function in the DS26521.
A7	H2TCS1	HDLC #2 transmit channel select 1		Unsupported function in the DS26521.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	DS26521 Bit Location 2155 Bit = 26521 Reg. Bit	Comments
A8	H2TCS2	HDLC #2 transmit channel select 2		Unsupported function in the DS26521.
A9	H2TCS3	HDLC #2 transmit channel select 3		Unsupported function in the DS26521.
AA	H2TCS4	HDLC #2 transmit channel select 4		Unsupported function in the DS26521.
AB	H2TTSBS	HDLC #2 transmit Time-slot bits/Sa bits select		Unsupported function in the DS26521.
AC	H2RPBA	HDLC #2 receive packet bytes available		Unsupported function in the DS26521.
AD	H2TF	HDLC #2 transmit FIFO		Unsupported function in the DS26521.
AE	H2RF	HDLC #2 Receive FIFO		Unsupported function in the DS26521.
AF	H2TFBA	HDLC #2 transmit FIFO buffer available		Unsupported function in the DS26521.

BERT Functions

The DS26521 BERT functions are more full featured than on the DS2155, so direct register mapping is not possible. The DS26521 pseudorandom patterns are fully programmable over 32 bits, compared to the fixed set of pseudorandom patterns found in the DS2155. Also, large repetitive patterns up to 512 bytes can be loaded with an indirect register. The BERT register set for the DS2155 is shown below, but the DS26521 data sheet should be consulted for all BERT functions.

DS2155 Address	DS2155 Symbol	DS2155 Register Description	Comments
DB	BAWC	BERT alternating word count Rate	Consult DS26521 data sheet
DC	BRP1	BERT repetitive pattern Set register 1	Consult DS26521 data sheet
DD	BRP2	BERT repetitive pattern Set register 2	Consult DS26521 data sheet
DE	BRP3	BERT repetitive pattern Set register 3	Consult DS26521 data sheet
DF	BRP4	BERT repetitive pattern Set register 4	Consult DS26521 data sheet
E0	BC1	BERT control register 1	Consult DS26521 data sheet
E1	BC2	BERT control register 2	Consult DS26521 data sheet
E2		Unused	Unused
E3	BBC1	BERT bit count register 1	Consult DS26521 data sheet
E4	BBC2	BERT bit count register 2	Consult DS26521 data sheet
E5	BBC3	BERT bit count register 3	Consult DS26521 data sheet
E6	BBC4	BERT bit count register 4	Consult DS26521 data sheet
E7	BEC1	BERT error count register 1	Consult DS26521 data sheet
E8	BEC2	BERT error count register 2	Consult DS26521 data sheet
E9	BEC3	BERT error count register 3	Consult DS26521 data sheet
EA	BIC	BERT interface control register	Consult DS26521 data sheet
EB	ERC	Error-rate control register	Consult DS26521 data sheet
EC	NOE1	Number-of-errors 1	Consult DS26521 data sheet
ED	NOE2	Number-of-errors 2	Consult DS26521 data sheet
EE	NOEL1	Number-of-errors Left 1	Consult DS26521 data sheet
EF	NOEL2	Number-of-errors Left 2	Consult DS26521 data sheet

Features Exclusive to the DS26521

There are many new functions in the DS26521.

Transmit Side Synchronizer

The DS26521 has a basic synchronizer on the transmit side. This function allows the transmitter to align to the data stream present at TSER when there is no externally supplied frame sync signal available.

Register name: **TSYNCC**
Register description: **Transmit Synchronizer Control Register**
Register address: **18EH**

7	6	5	4	3	2	1	0
--	--	--	--	CRC4	TSEN	SYNCE	RESYNC
0	0	0	0	0	0	0	0

Bit 2 - Transmit Synchronizer Enable (TSEN)

0 = Transmit-side synchronizer disabled

1 = Transmit-side synchronizer enabled

Bit 3 - CRC4 Enable (RCRC4). E1 Mode Only

0 = Do not search for the CRC4 multiframe word

1 = Search for the CRC4 multiframe word

Register name: **TLS3**
Register description: **Transmit Latched Status Register 3 (Synchronizer)**
Register address: **192H**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	LOF	LOFD
0	0	0	0	0	0	0	0

Bit 0 – Loss-of-Frame Synchronization Detect (LOFD)

This is a latched bit which is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 1 - Loss of Frame (LOF)

A real-time status bit that indicates that the transmit-side synchronizer is searching for the synchronization pattern in the incoming data stream.

Other Functions Exclusive to the DS26521

Register name: **GTCR1**
Register description: **Global Transceiver Control Register 1**
Register address: **0F0H**
Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	RLOFLTS	GIBOE	--	--	GCLE	GIPI
0	0	0	0	0	0	0	0

Bit 0 - Global Interrupt Pin Inhibit (GIPI)

0 = Normal operation. Interrupt pin (INT) will toggle low on an unmasked interrupt condition.
1 = Interrupt inhibit. Interrupt pin (INT) is forced high (inactive) when this bit is set.

Bit 1 - Global Counter Latch Enable (GCLE)

A low-to-high transition on this bit will, when enabled, latch the framer performance monitor counters. Each framer can be independently enabled to accept this input. This bit must be cleared and set again to perform another counter latch.

Bit 4 - Ganged IBO Enable (GIBOE)

This bit is used to select either the internal mux for IBO operation or an external "wire-OR" operation. Usually, this bit should be set = 0 and the internal mux used.
0 = Use internal IBO mux.
1 = Externally wire-OR. TSERs and RSERs for IBO operation.

Bit 5 – Receive Loss of Frame/Loss of Transmit Clock Indication Select (RLOFLTS)

0 = RLOF/LOTCx pins indicate framer receive loss of frame.
1 = RLOF/LOTCx pins indicate framer loss of transmit clock.

Register name: **GFCR**
Register description: **Global Framer Control Register**
Register address: **0F1H**
Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	BPCLK1	BPCLK0	RFLOSSFS	RFMSS	TCBCS	RCBCS
0	0	0	0	0	0	0	0

Bit 0 - Receive Channel Block/Clock Select (RCBCS)

This bit controls the function of all eight RCHBLK/CLK pins.
0 = RCHBLK/CLK pins output RCHBLK (1-8) (Receive Channel Block)
1 = RCHBLK/CLK pins output RCHCLK (1-8) (Receive Channel Clock)

Bit 1- Transmit Channel Block/Clock Select (TCBCS)

This bit controls the function of all eight TCHBLK/CLK pins.
0 = TCHBLK/CLK pins output TCHBLK (1-8) (Transmit Channel Block)
1 = TCHBLK/CLK pins output TCHCLK (1-8) (Transmit Channel Clock)

Bit 2 - Receive Frame/Multiframe Sync Select (RFMSS)

This bit controls the function of all eight RM/RFSYNC pins.
0 = RM/RFSYNC pins output RFSYNC (1-8) (Receive Frame Sync)
1 = RM/RFSYNC pins output RMSYNC (1-8) (Receive Multi-Frame Sync)

Bit 3 - Receive Loss of Signal / Signaling Freeze Select (RLOSSFS)

This bit controls the function of all eight AL/RSIGF/FLOS pins. The Receive LOS is further selected between Framer LOS and LIU LOS by GTCR2 Bit 2.
0 = AL/RSIGF/FLOS pins output RLOS (1-8) (Receive Loss)
1 = AL/RSIGF/FLOS pins output RSIGF (1-8) (Receive Signaling Freeze)

Register name: **GTCR2**
 Register description: **Global Framer Control Register**
 Register address: **0F2H**
 Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	LOSS	TSSYNIOSEL	--
0	0	0	0	0	0	0	0

Bit 1 - Transmit System Synchronization I/O Select (TSSYNIOSEL)

If this bit is set to a 1, the TSSYNCIO is an 8kHz output synchronous to the BPCLK. This “frame pulse” can be used in conjunction with the backplane clock to provide IBO signals for a system backplane. If this bit is reset, TSSYNCIO is an input. An 8kHz frame pulse is required for transmit synchronization and IBO operation.

Bit 2 - LOS Selection (LOSS)

If this bit is set, the AL/RSIGF/FLOS pins can be driven with LIU loss and if reset by framer LOS . The selection of whether to drive AL/RSIGF/FLOS pins with LOS (analog or digital) or signaling freeze is controlled by GFCR bit 2. This selection affects all ports.

Register name: **GTCCR**
 Register description: **Global Transceiver Clock Control Register**
 Register address: **0F3H**
 Read/write function: **R/W**

7	6	5	4	3	2	1	0
BPREFSEL3	BPREFSEL2	BPREFSEL1	BPREFSEL0	BFREQSEL	FREQSEL	MPS1	MPS0
0	0	0	0	0	0	0	0

Bit 2 - Frequency Selection (FREQSEL)

In conjunction with the MPS[1:0] bits, selects the external MCLK frequency of the signal input at the MCLK pin of the DS26521.

0 = The external master clock is 2.048MHz or a multiple thereof.

1 = The external master clock is 1.544MHz or a multiple thereof.

Bit 3 – Backplane Frequency Select (BFREQSEL)

In conjunction with BPRFSEL[3:0] identifies the reference clock frequency used by the DS26521 backplane clock-generation circuit. Note that the setting of this bit should match the T1E1 selection for the LIU whose recovered clock is being used to generate the backplane clock.

0 = Backplane reference clock is 2.048MHz.

1 = Backplane reference clock is 1.544MHz.

Bit 7 to 4 - Backplane Clock Reference Selects (BPREFSEL[3:0])

These bits select which reference clock source will be used for BPCLK generation. The BPCLK can be generated from any of the LIU recovered clocks, an external reference, or derivatives of MCLK input. Consult the DS26521 datasheet for details.

Register name: **GLSRR**
 Register description: **Global LIU Software Reset Register**
 Register address: **0F5H**
 Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	LSRST1
0	0	0	0	0	0	0	0

Bit 0 - Channel 1 LIU Software Reset (LSRST1)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset LIU

Register name: **GFSRR**
 Register description: **Global Framer and BERT Software Reset Register**
 Register address: **0F6H**
 Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	FSRST1
0	0	0	0	0	0	0	0

Bit 0 - Channel 1 Framer and BERT Software Reset (FSRST1)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset Framer and BERT

Register name: **GFISR**
 Register description: **Global Framer Interrupt Status Register**
 Register address: **0F9H**
 Read/write function: **R**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	FIS1
0	0	0	0	0	0	0	0

The GFISR register reports the framer interrupt status for the T1/E1 framer. A logic one in the associated bit location indicates a framer has set its interrupt signal.

Bit 0 : Framer Interrupt Status 1(FIS1).

0 = Framer 1 has not issued an interrupt.

1 = Framer 1 has issued an interrupt.

Register name: **GBISR**
 Register description: **Global BERT Interrupt Status Register**
 Register address: **0FAH**
 Read/write function: **R**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	BIS1
0	0	0	0	0	0	0	0

Bit 0 - BERT Interrupt Status 1 (BIS1)

0 = BERT 1 has not issued an interrupt.

1 = BERT 1 has issued an interrupt.

Register name: **GLISR**
 Register description: **Global LIU Interrupt Status Register**
 Register address: **0FBH**

Read/write function: **R**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	LIS1
0	0	0	0	0	0	0	0

Bit 0 - LIU Interrupt Status 1 (LIS1)

0 = LIU 1 has not issued an interrupt.

1 = LIU 1 has issued an interrupt.

Register name: **GFIMR**
Register description: **Global Framer Interrupt Mask Register**
Register address: **0FCH**
Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	FIM 1
0	0	0	0	0	0	0	0

Bit 0 - Framer 1 Interrupt Mask (FIM1)

0 = Interrupt masked.

1 = Interrupt enabled.

Register name: **GBIMR**
Register description: **Global BERT Interrupt Mask Register**
Register address: **0FDH**
Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	BIM 1
0	0	0	0	0	0	0	0

Bit 0 - BERT Interrupt Mask 1 (BIM1)

0 = Interrupt masked.

1 = Interrupt enabled.

Register name: **GLIMR**
Register description: **Global LIU Interrupt Mask Register**
Register address: **0FEH**
Read/write function: **R/W**

7	6	5	4	3	2	1	0
--	--	--	--	--	--	--	LIM 1
0	0	0	0	0	0	0	0

Bit 0 - LIU Interrupt Mask 1 (LIM1)

0 = Interrupt masked.

1 = Interrupt enabled.

Register name: **T1RCR2**
Register description: **Receive Control Register 2**
Register address: **014H**

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

--	--	--	RSLC96	OOF2	OOF1	RAIIE	RD4RM
0	0	0	0	0	0	0	0

Bit 1 - Receive RAI Integration Enable (RAIIE)

The ESF RAI indication can be interrupted for a period not to exceed 100ms per interruption (T1.403). In ESF mode, setting RAIIE causes the RAI status from the DS26521 to be integrated for 200ms.

0 = RAI detects when 16 consecutive patterns of 00FF appear in the FDL.

RAI clears when 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL

1 = RAI detects when the condition has been present for greater than 200ms.

RAI clears when the condition has been absent for greater than 200ms.

Register name: **RCR3**
Register description: **Receive Control Register 3**
Register address: **083H**

7	6	5	4	3	2	1	0
IDF	--	RSERC	--	--	--	PLB	FLB
0	0	0	0	0	0	0	0

Bit 7 - Input Data Format (IDF)

0 = Bipolar data is expected at RPOS and RNEG (either AMI or B8ZS)

1 = NRZ data is expected at RPOS. The BPV counter will be disabled and RNEG will be ignored by the DS26521.

Register name: **RRTS1**
Register description: **Receive Real Time Status Register 1**
Register address: **0B0H**

7	6	5	4	3	2	1	0
--	--	--	--	RRAI	RAIS	RLOS	RLOF
0	0	0	0	0	0	0	0

Bit 0 - Receive Loss of Frame Condition (RLOF)

Set when the DS26521 is not synchronized to the received data stream.

Bit 1 - Receive Loss of Signal Condition (RLOS)

Set when 255 (or 2048 if RCR2.0 = 1) consecutive zeros have been detected at RPOS and RNEG.

Bit 2 - Receive Alarm Indication Signal Condition (RAIS)

Set when an unframed all-ones code is received at RPOS and RNEG.

Bit 3 - Receive Remote Alarm Indication Condition (RRAI)

Set when a remote alarm is received at RPOS and RNEG.

Register name: **RRTS3 -T1 Mode**
 Register description: **Receive Real Time Status Register 3**
 Register address: **0B2H**

7	6	5	4	3	2	1	0
--	--	--	--	LORC	LSP	LDN	LUP
0	0	0	0	0	0	0	0

Bit 0 - (T1 MODE) Loop-Up Code Detected Condition (LUP)

Set when the loop-up code as defined in the RUPCD1/2 register is being received.

(E1 MODE) Receive Distant MF Alarm Condition (RDMA)

Set when bit-6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Bit 1 - (T1 MODE) Loop-Down Code Detected Condition (LDN)

Set when the loop-down code as defined in the RDNCD1/2 register is being received.

(E1 MODE) V5.2 Link Detected Condition (V52LNK)

Set on detection of a V5.2 link identification signal (G.965).

Bit 2 - Spare Code Detected Condition (LSP)

Set when the spare code as defined in the RSCD1/2 registers is being received.

Bit 3 - Loss of Receive Clock Condition (LORC)

Set when the RCLK pin has not transitioned for one channel time.

Register name: **RLS4**
 Register description: **Receive Latched Status Register 4**
 Register address: **093H**

7	6	5	4	3	2	1	0
RESF	RESEM	RSLIP	--	RSCOS	1SEC	TIMER	RMF
0	0	0	0	0	0	0	0

RLS4.2 – One-Second Timer (1SEC)

Set every 1s interval, based on RCLK.

Register name: **RLS7 – T1 Mode**
 Register description: **Receive Latched Status Register 7**
 Register address: **096H**

7	6	5	4	3	2	1	0
--	--	RRAI-CI	RAIS-CI	RSLC96	RFDLF	BC	BD
0	0	0	0	0	0	0	0

Bit 3 - Receive SLC-96 Alignment Event (RSLC96)

Set when a valid SLC-96 alignment pattern is detected in the Fs bit stream, and the RSLCx registers have data available for retrieval. (Section 11.12)

Bit 5 - Receive RAI-CI Detect (RRAI-CI)

Set when an RAI-CI pattern has been detected by the receiver (see Section 11.5.1). This bit is active in ESF framing mode only, and will set only if an RAI condition is being detected (RRTS1.3). When the host reads (and clears) this bit, it will set again each time the RAI-CI pattern is detected (approximately every 1.1 seconds).

Register name: **ERCNT**
 Register description: **Error Counter Configuration Register**
 Register address: **086H**

7	6	5	4	3	2	1	0
1SECS	MCUS	MECU	ECUS	EAMS	FSBE	MOSCRF	LCVCRF
0	0	0	0	0	0	0	0

Bit 6 - Manual Counter Update Select (MCUS)

When manual update mode is enabled with EAMS, this bit can be used to allow the GLCE bit in GCR1 to latch all counters. This is useful for synchronously latching counters of multiple framers.

0 = MECU is used to manually latch counters.

1 = GLCE is used to manually latch counters.

Bit 7 – One-Second Select (1SECS)

When timed update is enabled by EAMS, setting this bit for a specific framer will allow that framer's counters to latch on the 1s reference from framer #1. Note that this bit should always be clear for framer #1.

0 = Use internally generated 1s timer.

1 = Use 1s timer from framer #1.

Register name: **RESCR**
 Register description: **Receive Elastic Store Control Register**
 Register address: **085H**

7	6	5	4	3	2	1	0
RDATFMT	RGCLKEN	-	RSZS	RESALGN	RESR	RESMDM	RESE
0	0	0	0	0	0	0	0

Bit 4 - Receive Slip Zone Select (RSZS)

This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1-to-E1 or E1-to-T1 conversion applications.

0 = Force a slip at 9 bytes or less of separation (used for clustered blank channels)

1 = Force a slip at 2 bytes or less of separation (used for distributed blank channels)

Register name: **T1RBOCC**
 Register description: **Receive BOC Control Register**
 Register address: **015H**

7	6	5	4	3	2	1	0
RBR	--	RBD1	RBD0	--	RBF1	RBF0	-
0	0	0	0	0	0	0	0

Bit 5, 4 - Receive BOC Disintegration Bits (RBD[1:0])

The BOC disintegration filter sets the number of message bits that must be received without a valid BOC in order to set the BC bit indicating that a valid BOC is no longer being received.

RBD1	RBD0	Consecutive message bits for BOC clear identification
0	0	16
0	1	32
1	0	48
1	1	64

Register name: **TIOCR**
 Register description: **Transmit I/O Configuration Register**
 Register address: **184H**

7	6	5	4	3	2	1	0
TCLKINV	TSYNCINV	TSSYNCINV	TSCLKM	TSSM	TSIO	TSDW	TSM
0	0	0	0	0	0	0	0

Bit 3 - TSSYNC Mode Select (TSSM)

Selects frame or multiframe mode for the TSSYNC pin.

0 = frame mode

1 = multiframe mode

Register name: **TLS1**
 Register description: **Transmit Latched Status Register**
 Register address: **190H**

7	6	5	4	3	2	1	0
TESF	TESEM	TSLIP	TSLC96	TPDV	TMF	LOTCC	LOTCL
0	0	0	0	0	0	0	0

Bit 4 – (T1 Mode Only) Transmit SLC96 Multiframe Event (TSLC96)

When enabled by TCR2.6, this bit sets once per SLC96 multiframe (72 frames) to alert the host that new data might be written to the TSLC1-TSLC3 registers.

Register name: **TESCR**
Register description: **Transmit Elastic Store Control Register**
Register address: **185H**

7	6	5	4	3	2	1	0
TDATFMT	TGCLKEN	--	TSZS	TESALGN	TESR	TESMDM	TESE
0	0	0	0	0	0	0	0

Bit 4 - Transmit Slip Zone Select (TSZS)

This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit only affects the elastic stores when used in T1-to-E1 or E1-to-T1 conversion applications.

0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)

1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Conclusion

This application note shows the differences between the DS2155 and the DS26521 transceivers. It presents the terminology, the register mapping, and the features exclusive to the DS26521.

If you have further questions about our T1/E1 products, please contact the Telecommunication Applications support team by email at telecom.support@dalsemi.com, or call 972-371-6555