

APPLICATION NOTE 3630

Power Supply and Ground Design for a WiFi Transceiver

Abstract: A solid RF layout begins with understanding the fundamentals of board stack-up, supply routing, and grounding. This discussion addresses these fundamentals, and offers some practical, design-proven guidelines on power supply routing, supply bypassing, and grounding techniques to maximize the performance of any RF design. A practical example of controlling PLL spur levels is discussed, as PLL spurs are particularly sensitive to supply decoupling, grounding, and filter component placement. The MAX2827 802.11a/g transceiver reference design PCB layout is used for illustration.

Part 1: Fundamentals of Supply Routing and Bypassing

When designing RF circuits, the implementation and layout of the power supply section are often treated as an afterthought to the high-frequency signal path. Without careful consideration, it is easy for the supply voltages around the circuit to become corrupted and noisy, thus adversely affecting the system performance of the RF circuitry. Proper planning of the PCB layer stack-up, V_{CC} routing with a star topology, and proper decoupling of the V_{CC} pins will help achieve the best RF performance possible.

Starting with a sensible PCB layer definition will ease the remaining layout process. Given a four-layer board, as is commonly used in WLAN routing, a typical stack-up would use the top layer for component placement and RF routing, a ground plane on the second layer, power routing on the third layer, and whatever signal routing remains on the fourth layer. Placing an uninterrupted ground plane on the second layer is imperative for establishing well controlled impedances for the RF signal paths. It also allows the ground returns to be as short as possible and isolates the first and third layers so that coupling is minimized. While one can effectively use other stack-up approaches (required if a different number of layers is used), the approach presented here has proven successful.

While it may be tempting to use a large power plane to simplify the routing of the V_{CC} signals, this approach will most definitely lead to degraded system performance. By tying all the supply voltages together at a large plane, it is impossible to prevent noise transfer from one pin to another. Instead, using a star topology reduces coupling between the various supply pins in a system. An example of distributing V_{CC} through a star topology is shown in

Figure 1, taken from the layout of the MAX2826 IEEE 802.11a/g transceiver evaluation board. A main V_{CC} node is established, from which individual traces branch out to feed each RF IC supply pin. Using independent traces for each supply pin presents spatial separation between the pins, thus minimizing the amount of coupling that is seen. Each line will also have a finite amount of parasitic inductance associated with it, and works to help filter high-frequency noise from line.

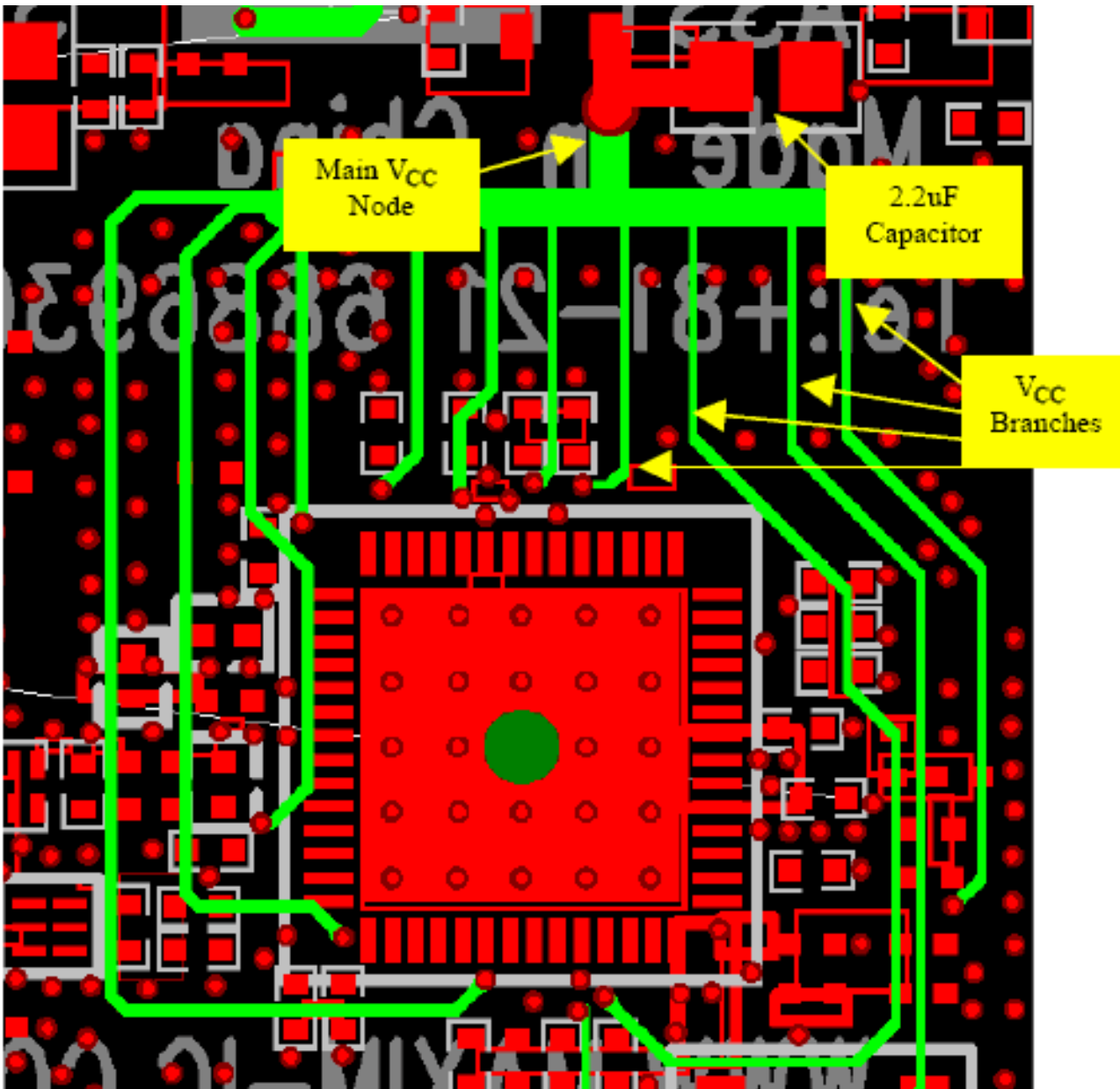


Figure 1. Star topology V_{CC} routing.

When using a star topology for V_{CC} routing, it is necessary to properly decouple the supply lines. Decoupling is complicated by the fact that capacitors have parasitic inductance. In practice, a capacitor is represented as a series RLC circuit as shown $f_s = \frac{1}{2\pi\sqrt{LC}}$. The capacitance will dominate at low frequencies, but after the self-resonant frequency (SRF) at $f_s = \frac{1}{2\pi\sqrt{LC}}$, the impedance of the capacitor will begin to look inductive. Thus, a capacitor is only useful for decoupling purposes over a frequency range that is near or below its SRF, where the capacitor presents a low impedance at the frequency of interest. **Figure 3** shows typical S11 performance for various capacitor values. From these plots, the SRFs can clearly be seen by the dip in the graph. It can also be seen that the higher capacitances provide better decoupling (appear lower impedance) at lower frequencies than do the lower valued capacitors.

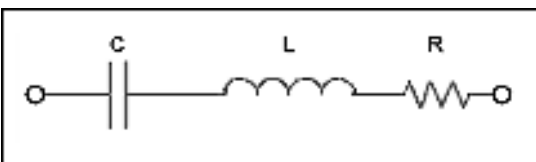


Figure 2. Equivalent circuit of a capacitor.

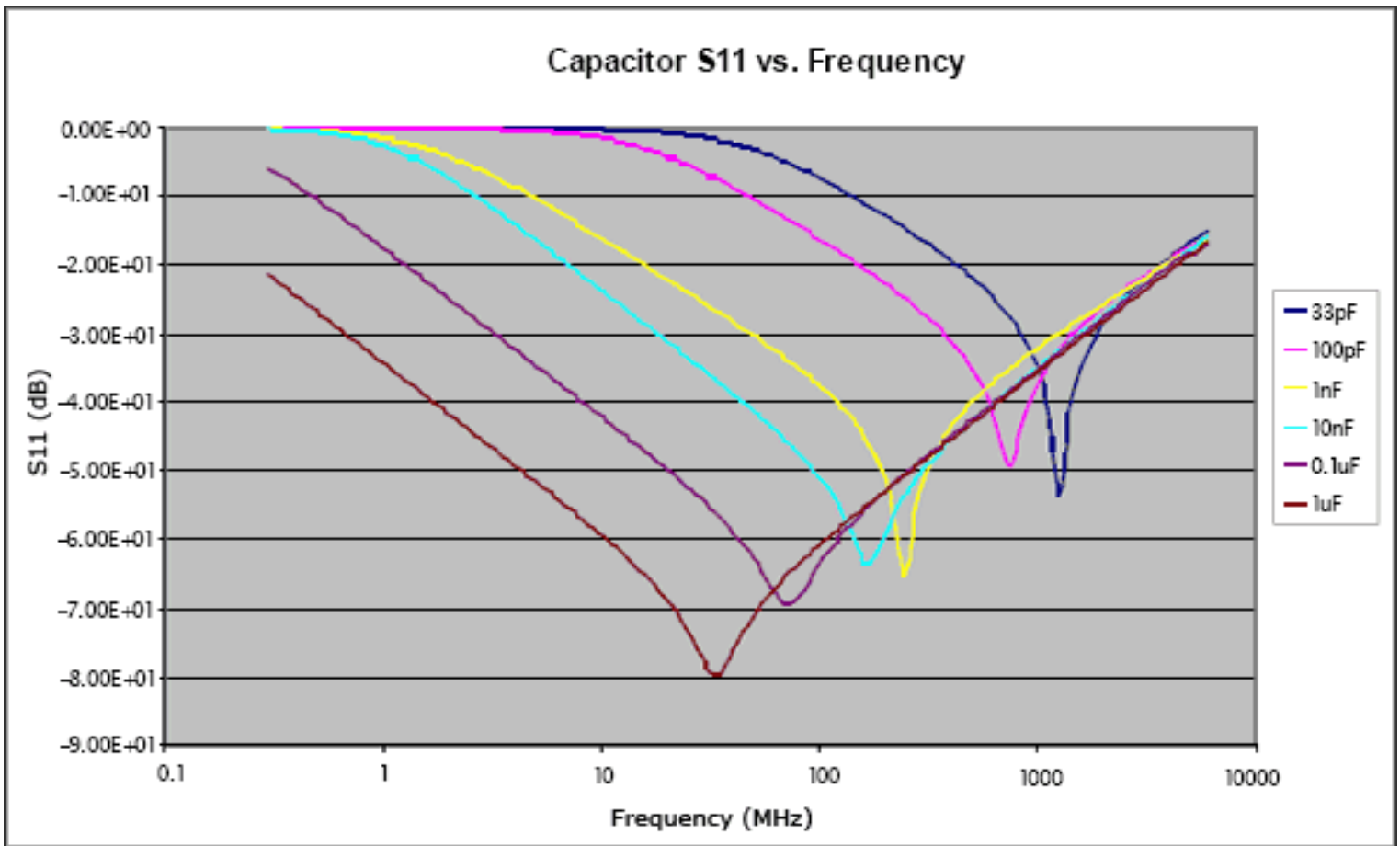


Figure 3. Capacitor impedance variations over frequency.

At the main node of the V_{CC} star, it is desirable to place a large-valued capacitor, such as $2.2\mu\text{F}$. This capacitor has a low SRF but is very effective at removing low-frequency noise and creating a stable DC voltage. At each supply pin of the IC, a lower valued capacitor, such as 10nF , should be used to remove any higher frequency noise that may couple onto the V_{CC} line. If the part of the circuit which the supply pin is powering is particularly sensitive to noise (i. e., a VCO supply), it may be necessary to place two capacitors close to the IC. Using a 100pF cap in parallel with a 10nF capacitor, for example, will provide a wider frequency range of decoupling and will thus make the supply less susceptible to noise. Each supply pin should be carefully examined to determine how much decoupling is necessary and at what frequencies the particular circuitry is most vulnerable to noise.

Combining good power supply decoupling techniques with a well-thought-out PCB layer stack-up and careful V_{CC} routing (implementing a star-topology) will provide a solid foundation for any RF system design. While there are many other factors that can still degrade system performance, having as noise-free a supply as possible is essential for achieving optimal performance.

Part 2: Fundamentals of RF Grounding and Using Ground Vias

Grounding and routing are also critical steps in WLAN board layout and fabrication. These steps will directly impact board parasitic parameters that sometimes result in undesirable system performance. There are no unique solutions to ground distribution in RF board design; several approaches can achieve satisfactory system performance. Split ground planes or split traces can be utilized to separate analog and digital signals or to isolate high-current or high-heat-generating sections. Based on previous experience with WLAN board design, however, a single solid ground plane in a four-layer stack-up board works well. The general rule is to avoid cross-interference by using a ground plane to shield the RF section from other circuitry in the board. As described in Part 1 above, layer 2 is usually designated as ground plane, while layer 1 is used for components and RF routing.

After grounding arrangements are settled, it is important to route all signal ground returns to the solid ground plane in the shortest path possible. Dropping vias from the top-layer ground to the ground plane is a common solution for this task. However, vias are quite inductive. The physical model of a via is shown in **Figure 4**. An accurate electrical model is given in **Figure 5**, where L_{via} is via inductance and C_{via} is parasitic capacitance of the PCB pad of a via. In

the grounding technique discussed here, the parasitic capacitance can be neglected. A 1.6mm deep via with a diameter of 0.2mm offers about 0.75nH inductance. The equivalent reactance at 2.5GHz/5.0GHz WLAN bands is about $12\Omega/24\Omega$ respectively. Therefore, a single via to ground does not provide real grounding for RF signals. In a good board design, drop as many vias to ground as possible in the RF circuitry section, especially for the exposed grounding paddle of popular IC packages. Failure to do this will, for example, cause undesirable emitter degeneration to occur in receive front-end or power-amplifier circuitry, which will result in diminished gain and degraded noise figure performance. It should be noted that a poorly soldered ground paddle will cause similar problematic effects. In addition, heat dissipation for power amplifiers requires many vias to a solid ground plane.

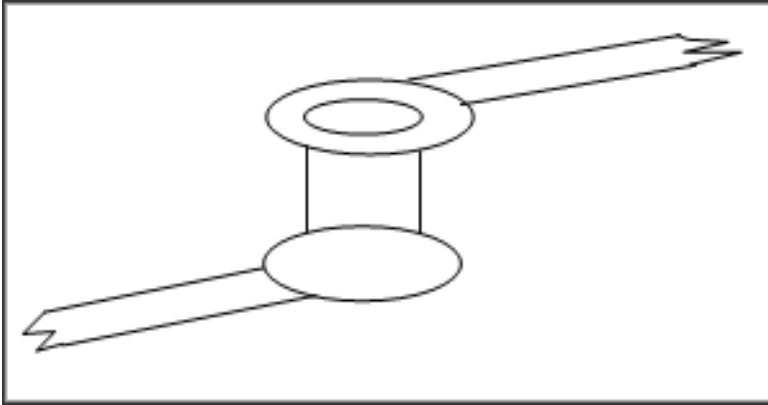


Figure 4. Physical model of via.

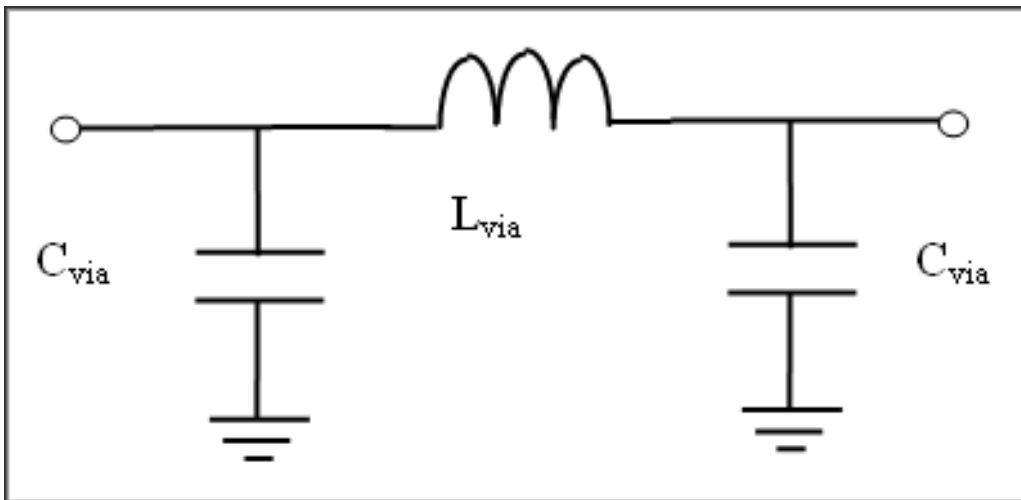


Figure 5. Electrical model of via.

Filtering noise from other stages, and constraining locally generated noise to avoid cross-interference between stages through V_{CC} lines are a few of the advantages of using V_{CC} decoupling. If the decoupling capacitors share the same ground vias, these vias at the joint end will carry all RF interference from both supplies due to the via inductance to ground. This not only makes decoupling capacitors lose their function, but also provides another path for noise coupling between stages in the system.

As discussed later in Part 3, PLL implementation always presents a challenge in system design. Satisfactory spur level performance may not be achieved without good grounding separation. In today's IC designs, all PLLs and VCOs are integrated into the chip; most PLLs utilize digital current-charge-pump outputs to control the VCO through a loop filter. Usually, a second- or third-order RC loop filter is required to filter the charge pump's digital pulse current to an analog control voltage. The two capacitors nearest the charge pump output must be grounded directly to the charge pump circuitry ground. This isolates the ground-return pulse-current path from the VCO ground, thus minimizing the comparison frequency spurs on the LO. The third capacitor (for a third-order filter) should directly connect to the VCO ground to prevent control voltages from floating with the digital current. Straying from these principals increases the risk of high comparison spurs.

An example of a PCB layout for grounding is shown in **Figure 6**. There are many ground vias in the grounding paddle, allowing each V_{CC} decoupling capacitor to have its own ground via. The circuitry within the box is the PLL loop filter. The first capacitor directly connects to GND_CP, while the second capacitor (in series with an R) turns 180 degrees and returns at the same GND_CP. The third capacitor, however, connects to GND_VCO. This ground distribution yields superior system performance.

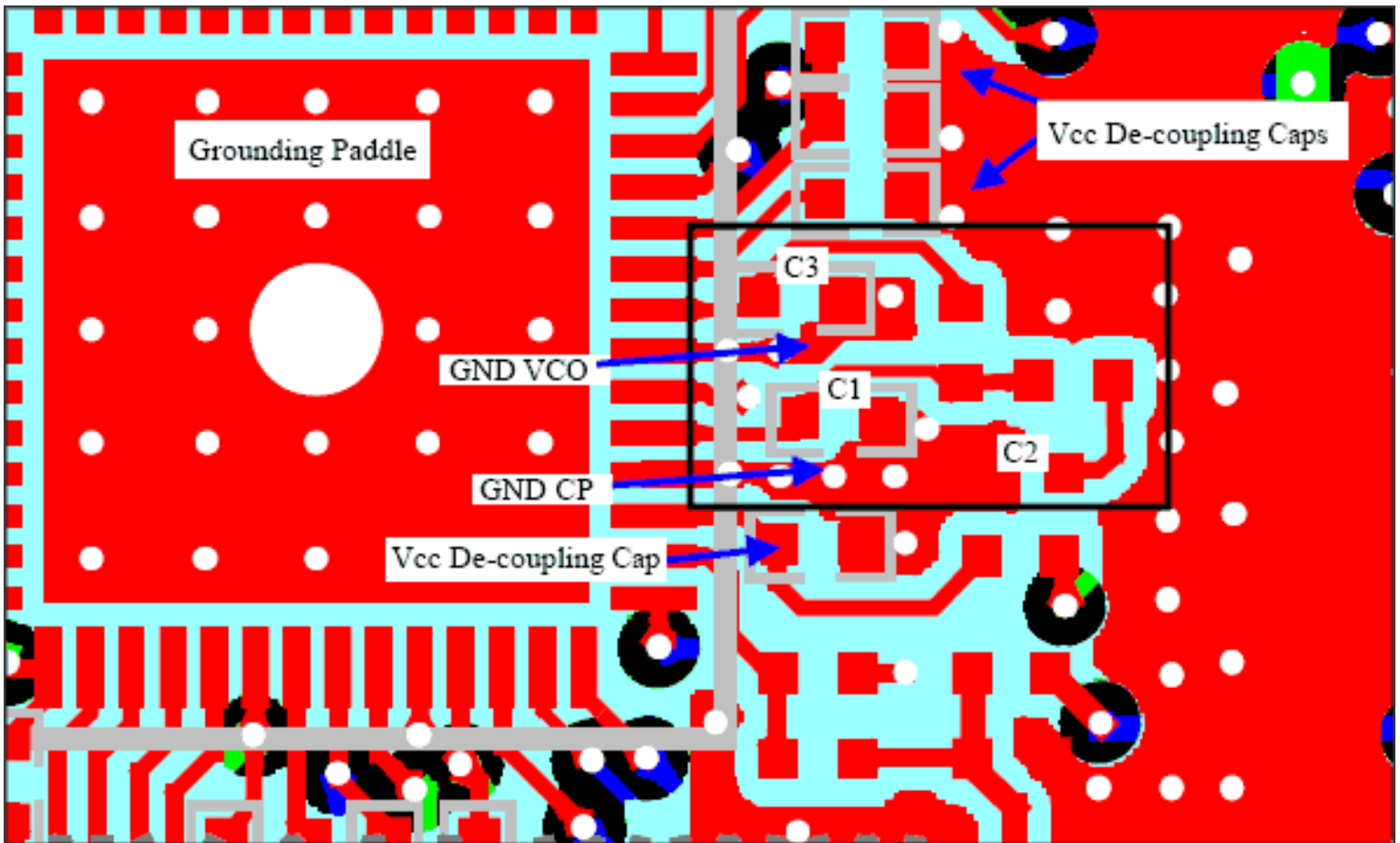
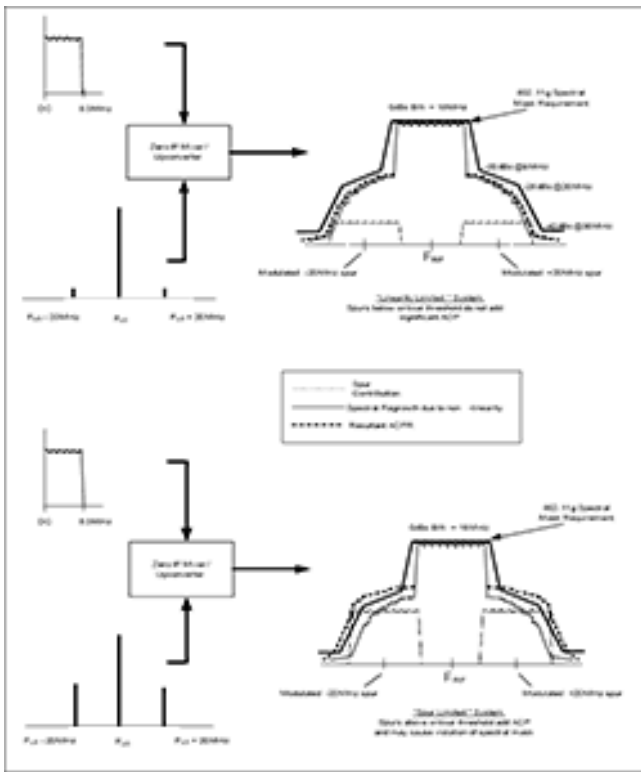


Figure 6. Example of PLL filter-component placement and grounding, as on the MAX2827 reference design board.

Part 3: Managing PLL Spurious with Proper Supply Bypassing and Grounding

Meeting transmit spectral-mask requirements in an 802.11a/b/g system can be a challenging component of the design process as well. Linearity and power consumption must be balanced with enough margin to fall within IEEE and FCC specifications while maintaining adequate transmit output power. A typical target for an IEEE 802.11g system is +15dBm at the antenna and -28dBr at 20MHz offset. In-band Adjacent Channel Power Ratio (ACPR) is considered largely a function of a device's linearity, which can be adapted within reason, to a particular application. The arduous task of optimizing ACPR in transmit line-ups is most often accomplished empirically through bias adjustments in both Tx IC and PA, coupled with fine-tuning of PA input, output, and interstage matching networks.

However, not all apparent ACPR issues are necessarily due to device linearity. In a prime example, a WLAN transmitter can exhibit less than desirable adjacent channel performance even after extensive tuning and optimization of both the power amplifier and PA driver (two of the main contributors to ACPR). Spurs on the Local Oscillator (LO) from the transmitter's Phase-Locked Loop (PLL) can also cause poor ACPR performance. The LO spurs will mix readily with the modulated baseband signal and the product will be amplified along with the desired channel (see **Figure 7**). This mixing action is only an issue when the PLL spurs are above a certain threshold. When they are below this threshold, the ACPR will be dominated by PA nonlinearities. When the Tx output power and spectral mask performance are 'linearity limited,' we can trade-off current for linearity and output power, which is the desired scenario. If LO spurs dominate the ACPR performance, then we are 'spur limited' and required to bias the PA higher to keep its ACPR contribution down for a given P_{OUT} . This latter solution needs more current and offers less flexibility in the design.



[For Larger Image](#)

Figure 7. 802.11g spectral mask requirements and the degradation from comparison spurs.

This situation leads one to question how to efficiently limit PLL spurs to an amplitude that does not influence the transmit spectrum? A few techniques can be used once the offending spur has been identified. The first and most tempting solution may be to narrow the PLL's loop-filter bandwidth in an attempt to attenuate the spur. This can work in a few select cases, but an example will expose the potential folly of this line of reasoning.

Take, for instance, the hypothetical situation presented in **Figure 8**. Suppose a fractional-N synthesizer with a 20MHz comparison frequency is used. If the loop filter is second-order with a cutoff frequency of 200kHz, a roll-off of roughly 40dB/decade is nominal, yielding 80dB of attenuation at 20MHz. If the reference spur is measured at -40dBc, a level that is likely to cause undesired modulation, the mechanism causing the spur will probably occur beyond the influence of the loop filter. (If it were generated prior to the filter, it would have been *extremely* strong from the beginning). Narrowing the filter bandwidth is not likely to improve this spur, but will increase PLL lock-time—a decidedly undesirable effect.

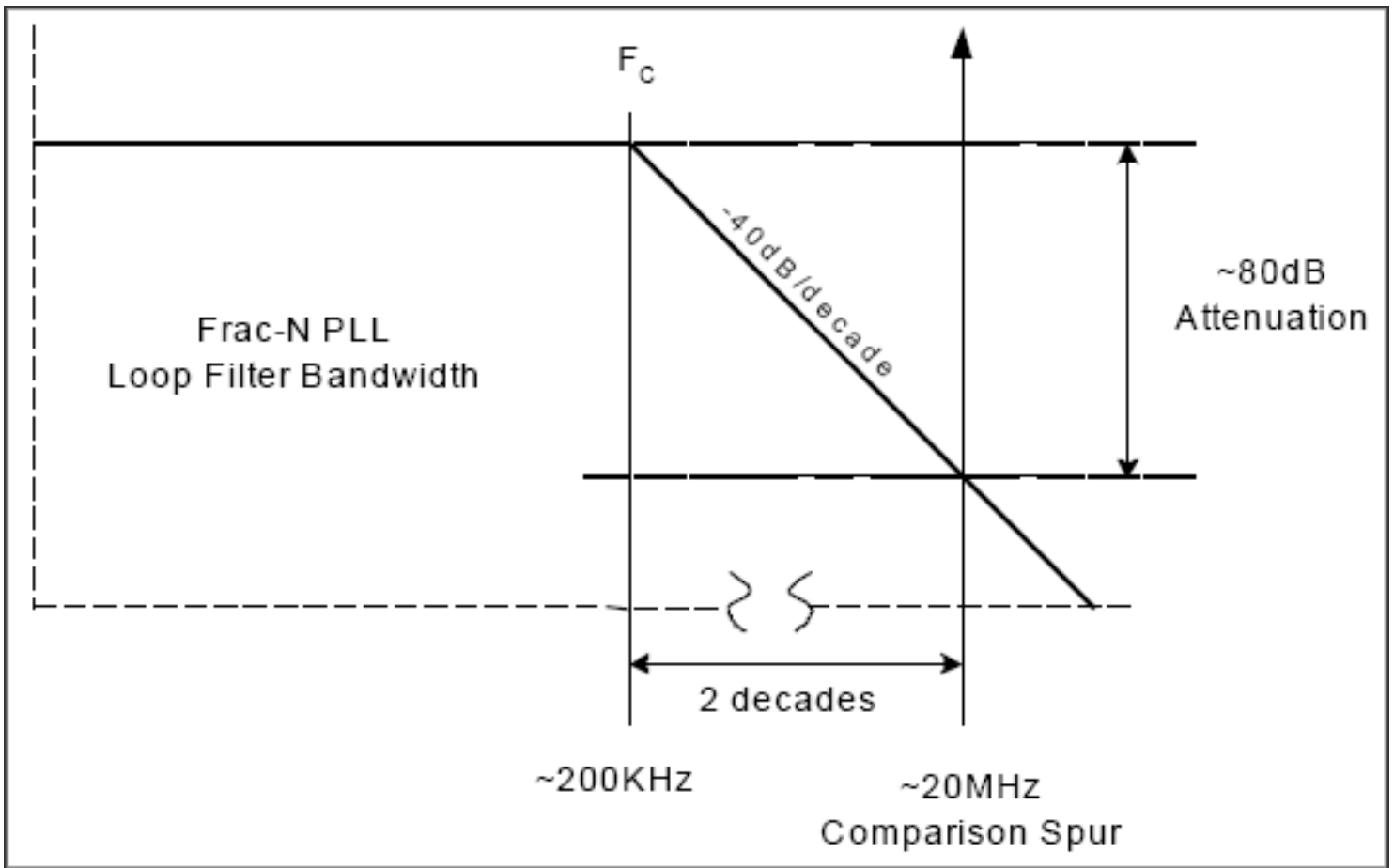


Figure 8. Simplified PLL filter asymptotes, and relative placement of corner frequency and comparison spur.

Arguably, the most effective way to combat PLL spurs is by utilizing appropriate grounding, power supply routing, and decoupling techniques. The items discussed at the beginning of this article are a good starting point to mitigate PLL spur issues. A star topology is imperative here due to the relatively large current changes that occur in the charge pump. The noise generated by current pulses can couple to the power supply of the VCO if isolation is not adequate, and will effectively modulate the VCO at the comparison frequency. This is commonly known as 'VCO pushing.' Isolation can be improved through physical separation of the power supply lines, decoupling at each V_{CC} pin, judicious placement of ground vias, and introduction of series ferrite elements (consider as a last resort). While not all these measures may be necessary in every design, each can be used as part of a larger spur mitigation strategy.

Figure 9 demonstrates the effect an inadequately decoupled VCO power supply. The supply ripples shown directly relate to charge-pump activity that is corrupting the supply line. Fortunately in this case, the corruption could be reduced significantly by increasing the local bypass capacitance. **Figure 10** was measured at the same point after the change.

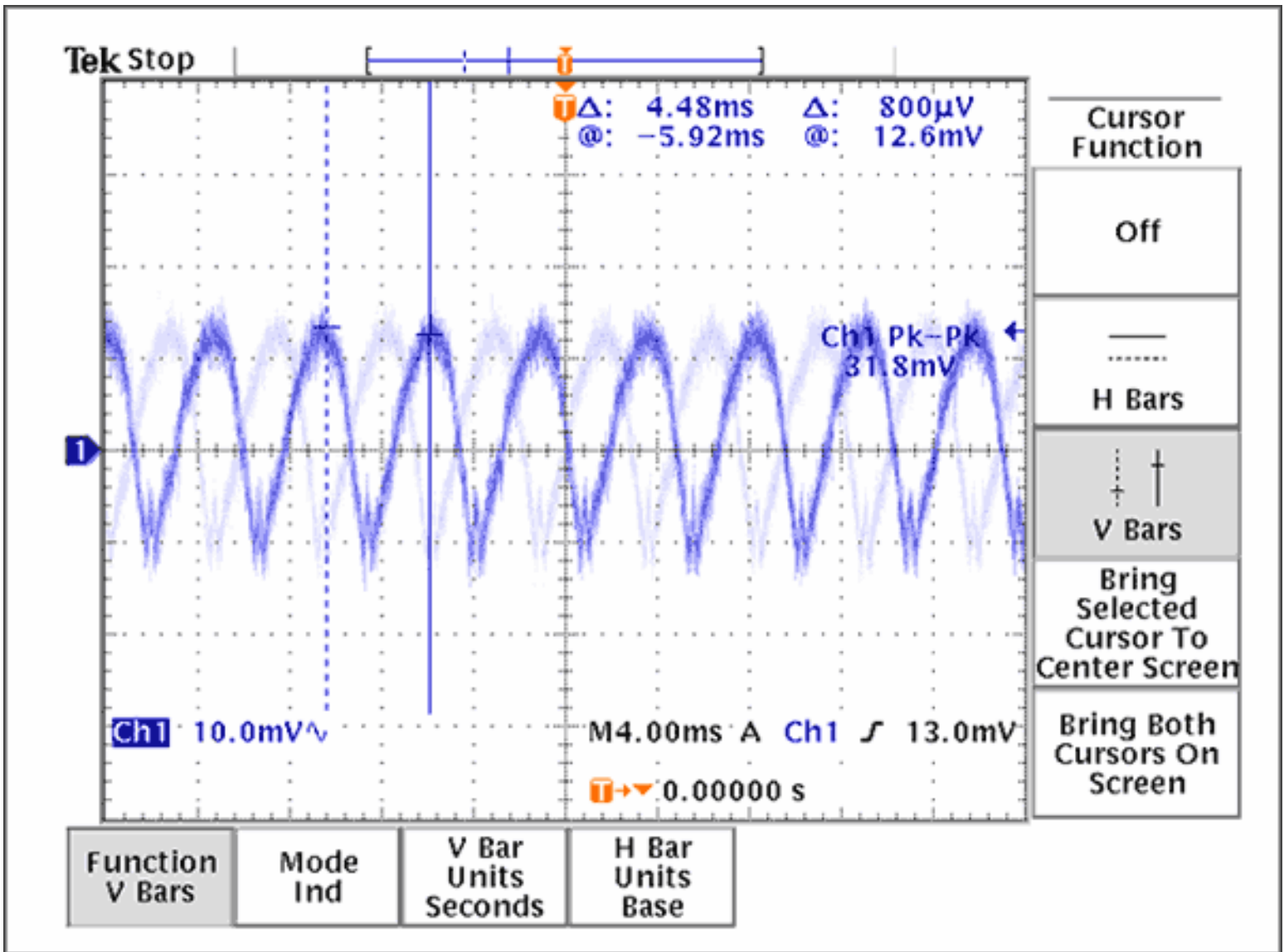


Figure 9. An inadequately decoupled VCC_VCO.

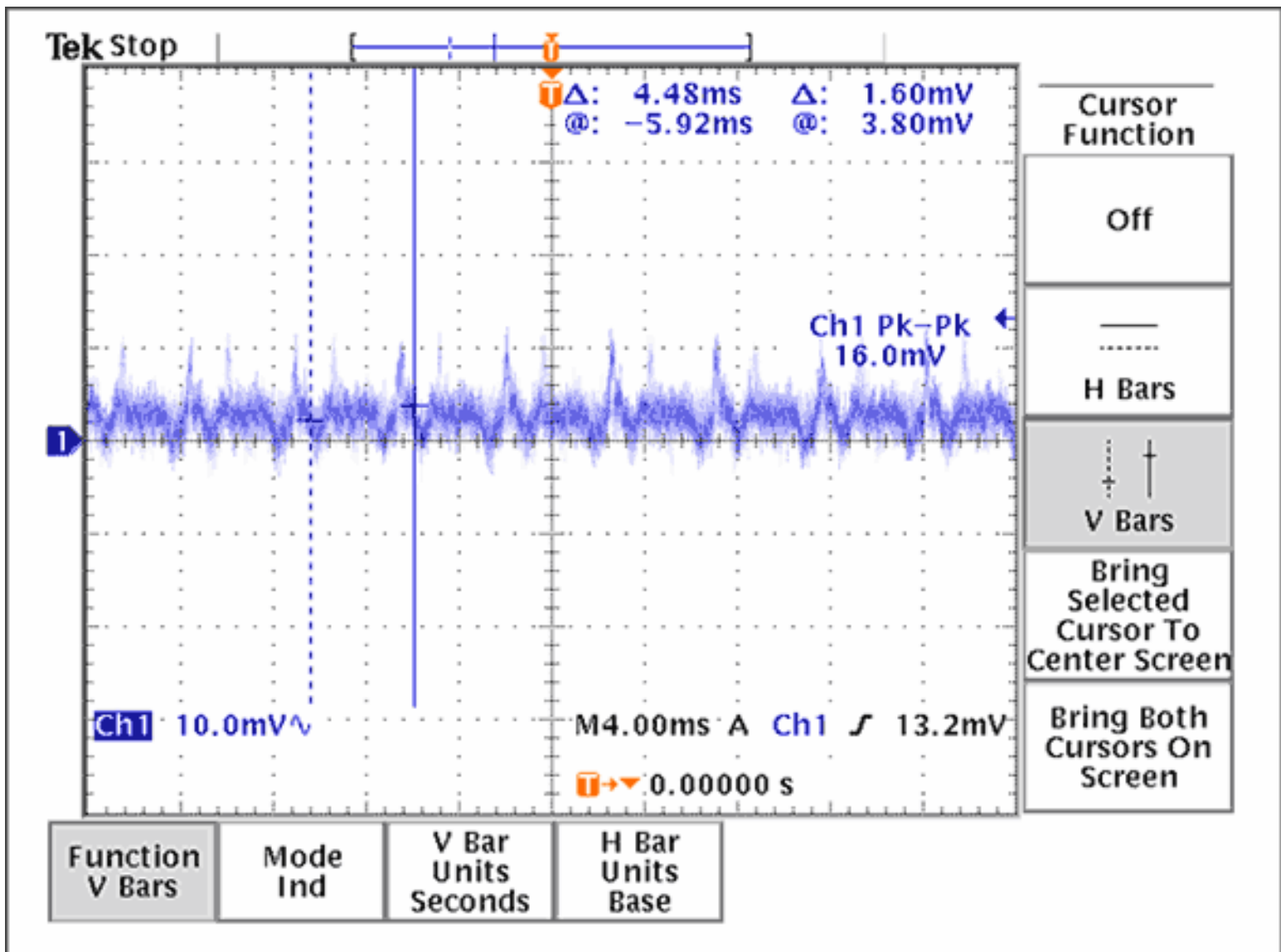


Figure 10. Increased bypass capacitance at the VCO supply quiets the noise.

In another example, similar noise was observed on the VCO supply. The resultant spurs were strong enough to influence ACPR and no amount of decoupling improved the situation. In this case, a review of the PCB layout revealed that the VCO supply trace was run directly beneath the charge-pump supply. Rerouting the trace reduced the spur to a spec-compliant level.

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