

APPLICATION NOTE 3623

## Battery-Charger PWM Input Has Watchdog Protection

*Abstract: Adding watchdog protection to the charger-input circuitry of a mobile phone guards against damage when the baseband processor stalls or ceases software execution.*

Mobile-phone batteries are usually charged through a proprietary charging algorithm in the baseband controller. The phone's charger input is connected to the internal battery through a p-channel switch of low on-resistance, controlled by a pulse-width modulation (PWM) signal from the baseband controller (**Figure 1**). To minimize power dissipation and consequent thermal problems in the phone, the charging supply (usually a wall cube) is current limited and specified according to the battery's chemistry and charge-recovery requirements.

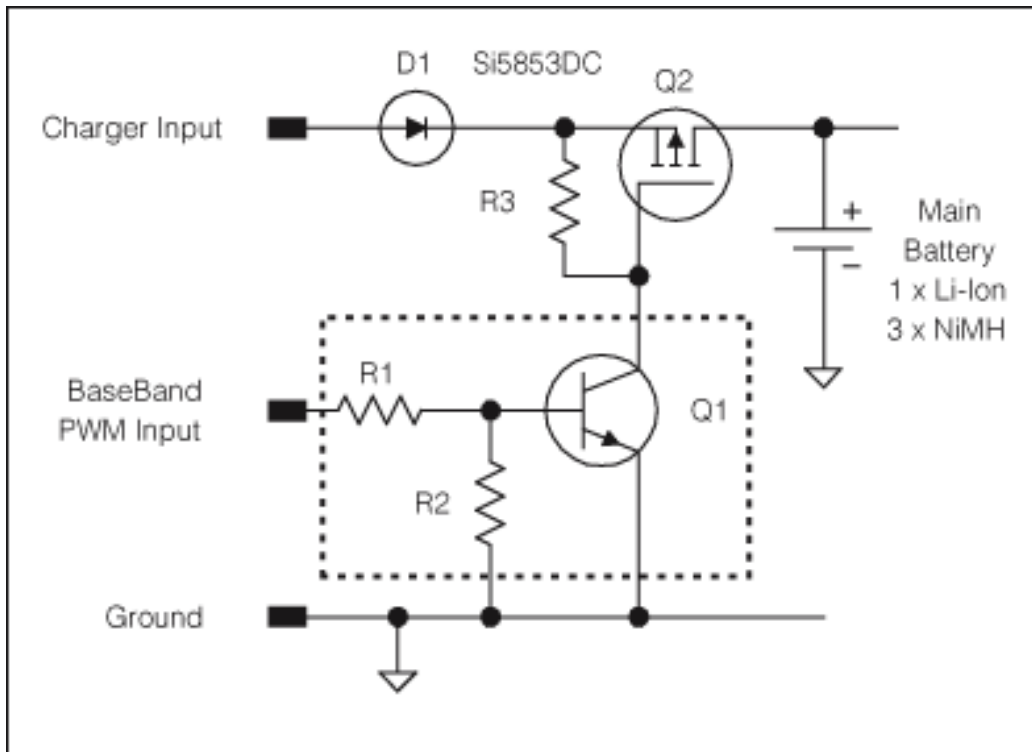


Figure 1. Typical charger-input circuitry for a mobile phone.

Note that the (almost) direct connection between charger and battery could cause damage if the baseband processor should stall for any reason. What is needed is a circuit that monitors the PWM input and disables the series power switch after a predetermined delay interval. The circuit should be independent of the processor, and should allow charging to restart when the PWM signal returns.

To provide this protection, add a microprocessor supervisor (one that includes a watchdog circuit for software execution) and a usually open, SPST analog switch (**Figure 2**). The two ICs shown are available in 5-lead SOT23 packages to minimize space. R4, D2, and C1 protect the ICs by limiting  $V_{CC}$  to a maximum of 5.1V. The R4 value isn't critical, because quiescent current for the added circuit is very low (30 $\mu$ A). Choose the R4 value to provide just enough current (0.5mA) to activate the Zener diode's "knee" characteristic.

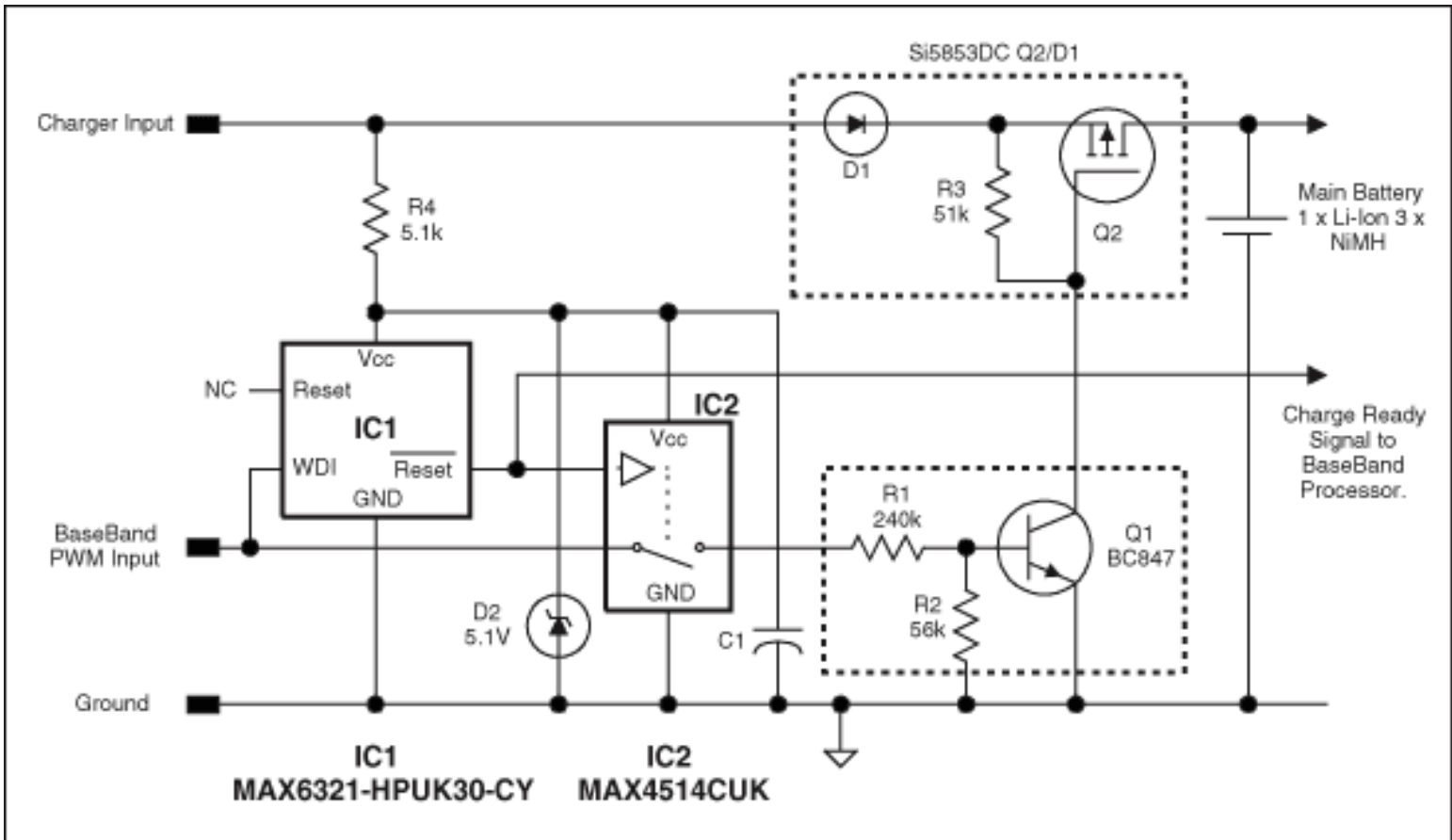


Figure 2. Adding watchdog protection to the circuit in Figure 1 guards against damage when the baseband processor stalls or ceases software execution.

The protection circuit doesn't burden the battery, because it receives no power except when the battery is being charged. The /RESET\ output produces a /CHARGER READY\ interrupt to the baseband controller CPU, and the open-drain structure of /RESET\ allows connection to other circuitry operating from different supply voltages. Powering the watchdog and PWM circuit only while charging also prevents a reverse discharge into /RESET\.

Circuit operation begins when an active charger is connected to the charger-input socket. When  $V_{CC}$  reaches  $3V \pm 45mV$  (in this example, using a 3V trim), the Reset period begins. Two hundred milliseconds later, Reset goes low and /Reset\ goes high (for the CY-suffix version of IC1). /Reset\ releases the SPST analog switch IC2, which enables the PWM input. At the same time, the active watchdog input (WDI) monitors the PWM input signal. If that signal does not produce a transition within 1.6 seconds (for the CY-suffix version of IC1), the RESET and /RESET\ outputs become active, disable the PWM input, and pause the charger algorithm through a CPU interrupt conveyed by the Charger Ready signal.

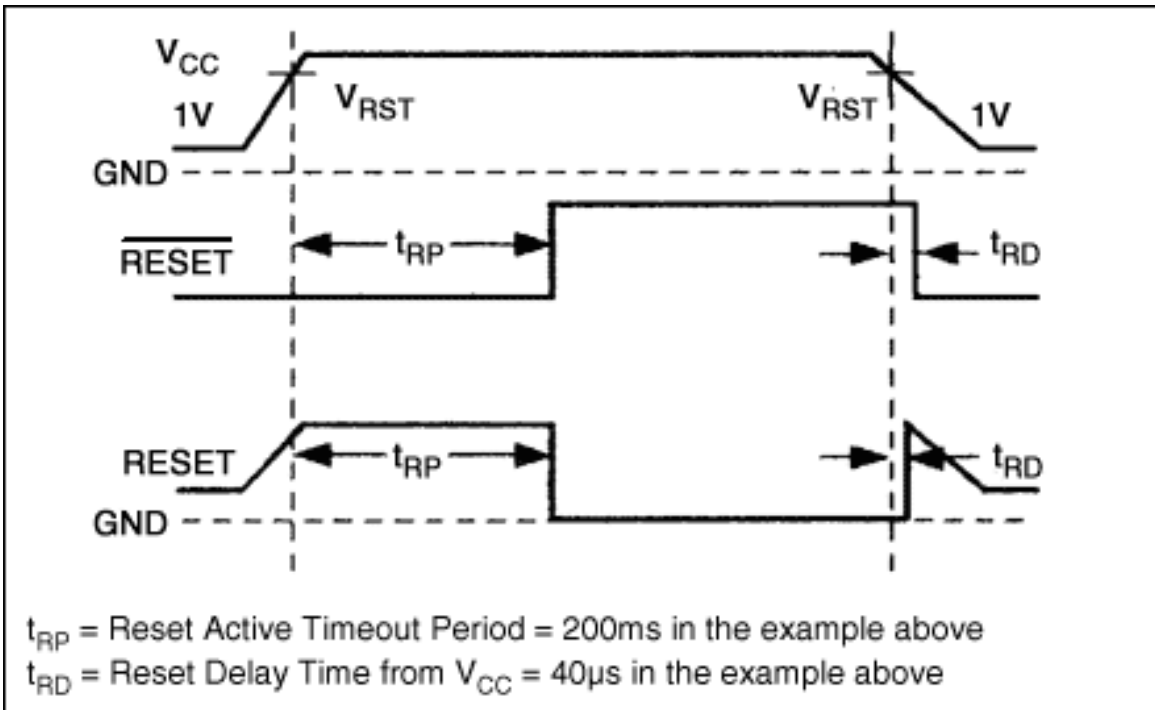


Figure 3. Reset-timing relationships for the Figure 2 circuit.

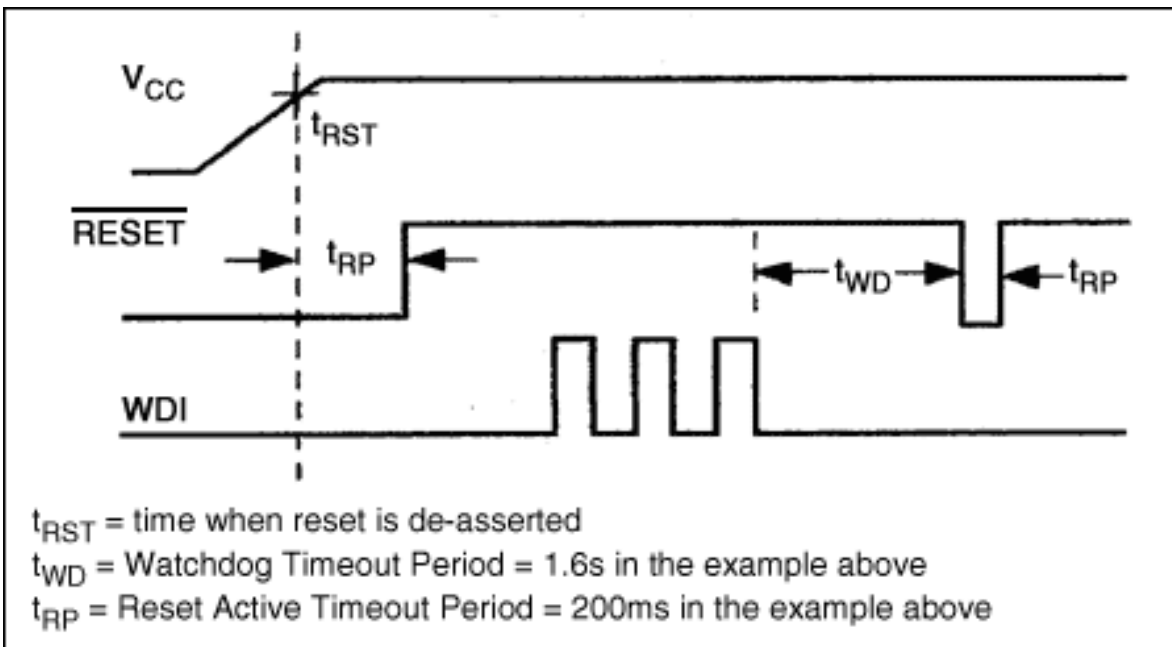


Figure 4. Timing relationships for the watchdog input in Figure 2.

This design idea appeared in the July 21, 2005 issue of EDN.

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