

APPLICATION NOTE 357

DS21Q42 vs. DS21Q41B

This application note describes the hardware and software differences between the Dallas Semiconductor DS21Q42 and the DS21Q41B quad port framer devices. The DS21Q42 enhanced quad T1 framer offers a broader feature set while retaining the original features of the DS21Q41B. As such, the designer must decide on what changes need to be made in software and hardware when migrating to the DS21Q42 from the DS21Q41B quad T1 framer. Any designer who is thinking of upgrading an existing design to use the DS21Q42 should read this application note. The application note contains detailed information for software migration such as: register location changes, how individual functions have changed from the DS21Q41B to the DS21Q42, and which new functions are available on the DS21Q42. It also covers migration for the hardware interface and covers new functions that are available in the DS21Q42. In the end, the designer should have enough information to easily migrate an existing design which uses the DS21Q41B to the DS21Q42 device.

Introduction

This application note highlights the differences between the DS21Q42 and the DS21Q41B Quad T1 Framers. The DS21Q42 is a superset of the DS21Q41B. The DS21Q42 is only offered in a 3.3 volt version with 5 volt tolerant I/O. All of the original features of the DS21Q41B have been retained and software created for the DS21Q41B is transferable to the DS21Q42 with minimal effort.

2.0 Additional Functionality

New Features	Data Sheet Section
Framer Mode Select (FMS) hardware pin provides DS21Q41B emulation mode	1
8.192 MHz clock synthesizer	1 & 3
CRC6 support for Japanese standard	6
Expanded receive and transmit elastic store reset functions	6
Device ID register	6
RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state	7
Loss of Receive clock indication	7
Ability to monitor one DSO channel in both the transmit and receive paths	9
Additional hardware signaling capability including: <ul style="list-style-type: none"> • Receive signaling re-insertion to a backplane multiframe sync • Signaling freezing 	10
Per-channel code insertion in both transmit and receive paths	11
Per-channel loopback	11
Ability to pass the F-Bit position through the elastic stores in the 2.048 MHz backplane mode	13

HDLC controller	
<ul style="list-style-type: none"> • 64-byte buffers • Configurable for FDL or DSO access 	14
Programmable inband code generation and detection	16
Interleaved PCM bus operation	18
TAG support	19
3.3V operation with 5V tolerant I/O	21

3.0 Changes in Register Definitions

When implementing the new features of the DS21Q42, a priority was placed on preserving the DS21Q41B's register map to facilitate code migration from existing DS21Q41B designs. This section highlights register additions and differences found in the DS21Q42.

3.1 Register Map Comparison

Address	R/W	DS21Q42 Register Name	DS21Q41B Register Name
00	R/W	FDL Control	Not Present
01	R/W	FDL Status	Not Present
02	R/W	FDL Interrupt Mask	Not Present
03	R/W	Receive Performance Report Message	Not Present
04	R/W	Receive Bit Oriented Code	Not Present
05	R	Receive FDL FIFO	Not Present
06	R/W	Transmit Performance Report Message	Not Present
07	R/W	Transmit Bit Oriented Code	Not Present
08	W	Transmit FDL FIFO	Not Present
09	R/W	Test Register	Not Present
0A	R/W	Common Control 7	Not Present
0B	—	Not Present	Not Present
0C	—	Not Present	Not Present
0D	—	Not Present	Not Present
0E	—	Not Present	Not Present
0F	R	Device ID	Not Present
10	R/W	Receive Information 3	Not Present
11	R/W	Common Control 4	Not Present
12	R/W	In-Band Code Control	Not Present
13	R/W	Transmit Code Definition	Not Present
14	R/W	Receive Up Code Definition	Not Present
15	R/W	Receive Down Code Definition	Not Present
16	R/W	Transmit Channel Control 1	Not Present
17	R/W	Transmit Channel Control 2	Not Present
18	R/W	Transmit Channel Control 3	Not Present
19	R/W	Common Control 5	Not Present

1A	R	Transmit DS0 Monitor	Not Present
1B	R/W	Receive Channel Control 1	Not Present
1C	R/W	Receive Channel Control 2	Not Present
1D	R/W	Receive Channel Control 3	Not Present
1E	R/W	Common Control 6	Not Present
1F	R	Receive DS0 Monitor	Not Present
20	R/W	Status 1	Same
21	R/W	Status 2	Bit Difference
22	R/W	Receive Information 1	Same
23	R	Line Code Violation Count 1	Same
24	R	Line Code Violation Count 2	Same
25	R	Path Code Violation Count 1	Same
26	R	Path Code Violation Count 2	Same
27	R	Multiframe Out of Sync Count 2	Same
28	R	Receive FDL Register	Same
29	R/W	Receive FDL Match 1	Same
2A	R/W	Receive FDL Match 2	Same
2B	R/W	Receive Control 1	Same
2C	R/W	Receive Control 2	Same
2D	R/W	Receive Mark 1	Same
2E	R/W	Receive Mark 2	Same
2F	R/W	Receive Mark 3	Same
30	R/W	Common Control 3	Bit Difference
31	R/W	Receive Information 2	Same
32	R/W	Transmit Channel Blocking 1	Same
33	R/W	Transmit Channel Blocking 2	Same
34	R/W	Transmit Channel Blocking 3	Same
35	R/W	Transmit Control 1	Same
36	R/W	Transmit Control 2	Same
37	R/W	Common Control 1	Same
38	R/W	Common Control 2	Same
39	R/W	Transmit Transparency 1	Same
3A	R/W	Transmit Transparency 2	Same
3B	R/W	Transmit Transparency 3	Same
3C	R/W	Transmit Idle 1	Same
3D	R/W	Transmit Idle 2	Same
3E	R/W	Transmit Idle 3	Same
3F	R/W	Transmit Idle Definition	Same
40	R/W	Transmit Channel 9	Not Present
41	R/W	Transmit Channel 10	Not Present
42	R/W	Transmit Channel 11	Not Present
43	R/W	Transmit Channel 12	Not Present

44	R/W	Transmit Channel 13	Not Present
45	R/W	Transmit Channel 14	Not Present
46	R/W	Transmit Channel 15	Not Present
47	R/W	Transmit Channel 16	Not Present
48	R/W	Transmit Channel 17	Not Present
49	R/W	Transmit Channel 18	Not Present
4A	R/W	Transmit Channel 19	Not Present
4B	R/W	Transmit Channel 20	Not Present
4C	R/W	Transmit Channel 21	Not Present
4D	R/W	Transmit Channel 22	Not Present
4E	R/W	Transmit Channel 23	Not Present
4F	R/W	Transmit Channel 24	Not Present
50	R/W	Transmit Channel 1	Not Present
51	R/W	Transmit Channel 2	Not Present
52	R/W	Transmit Channel 3	Not Present
53	R/W	Transmit Channel 4	Not Present
54	R/W	Transmit Channel 5	Not Present
55	R/W	Transmit Channel 6	Not Present
56	R/W	Transmit Channel 7	Not Present
57	R/W	Transmit Channel 8	Not Present
58	R/W	Receive Channel 17	Not Present
59	R/W	Receive Channel 18	Not Present
5A	R/W	Receive Channel 19	Not Present
5B	R/W	Receive Channel 20	Not Present
5C	R/W	Receive Channel 21	Not Present
5D	R/W	Receive Channel 22	Not Present
5E	R/W	Receive Channel 23	Not Present
5F	RW	Receive Channel 24	Not Present
60	R	Receive Signaling 1	Same
61	R	Receive Signaling 2	Same
62	R	Receive Signaling 3	Same
63	R	Receive Signaling 4	Same
64	R	Receive Signaling 5	Same
65	R	Receive Signaling 6	Same
66	R	Receive Signaling 7	Same
67	R	Receive Signaling 8	Same
68	R	Receive Signaling 9	Same
69	R	Receive Signaling 10	Same
6A	R	Receive Signaling 11	Same
6B	R	Receive Signaling 12	Same
6C	R/W	Receive Channel Blocking 1	Same
6D	R/W	Receive Channel Blocking 2	Same

6E	R/W	Receive Channel Blocking 3	Same
6F	R/W	Interrupt Mask 2	Bit Difference
70	R/W	Transmit Signaling 1	Same
71	R/W	Transmit Signaling 2	Same
72	R/W	Transmit Signaling 3	Same
73	R/W	Transmit Signaling 4	Same
74	R/W	Transmit Signaling 5	Same
75	R/W	Transmit Signaling 6	Same
76	R/W	Transmit Signaling 7	Same
77	R/W	Transmit Signaling 8	Same
78	R/W	Transmit Signaling 9	Same
79	R/W	Transmit Signaling 10	Same
7A	R/W	Transmit Signaling 11	Same
7B	R/W	Transmit Signaling 12	Same
7C	—	Not Present	Test Register
7D	R/W	Test Register	Test Register
7E	R/W	Transmit FDL Register	Same
7F	R/W	Interrupt Mask Register 1	Same
80	R/W	Receive Channel 1	Not Present
81	R/W	Receive Channel 2	Not Present
82	R/W	Receive Channel 3	Not Present
83	R/W	Receive Channel 4	Not Present
84	R/W	Receive Channel 5	Not Present
85	R/W	Receive Channel 6	Not Present
86	R/W	Receive Channel 7	Not Present
87	R/W	Receive Channel 8	Not Present
88	R/W	Receive Channel 9	Not Present
89	R/W	Receive Channel 10	Not Present
8A	R/W	Receive Channel 11	Not Present
8B	R/W	Receive Channel 12	Not Present
8C	R/W	Receive Channel 13	Not Present
8D	R/W	Receive Channel 14	Not Present
8E	R/W	Receive Channel 15	Not Present
8F	R/W	Receive Channel 16	Not Present
90	R/W	Receive HDLC DSO Control Register 1	Not Present
91	R/W	Receive HDLC DSO Control Register 2	Not Present
92	R/W	Transmit HDLC DSO Control Register 1	Not Present
93	R/W	Transmit HDLC DSO Control Register 2	Not Present
94	R/W	Interleave Bus Operation Register	Not Present
95	—	Not Present	Not Present
96	—	Not Present	Not Present
97	—	Not Present	Not Present

98	—	Not Present	Not Present
99	—	Not Present	Not Present
9A	—	Not Present	Not Present
9B	—	Not Present	Not Present
9C	—	Not Present	Not Present
9D	—	Not Present	Not Present
9E	—	Not Present	Not Present
9F	—	Not Present	Not Present

NOTE: Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all zeros) on power up initialization to insure proper operation.

3.2 New Feature Register Usage

Highlights specific registers containing bit locations related to new features. Each item can be found in the data sheet under the listed sections.

3.2.1 Device Identification (section 6)

Register	Description
IDR	Device Identification Register

3.2.2 Expanded Elastic Stores Reset Functions (section 6)

Register	Description
CCR5	Common Control 5
CCR6	Common Control 6

3.2.3 Loss of Receive Clock (section 6)

Register	Description
RIR3	Receive Information Register 3

3.2.4 Japanese CRC6 Mode (section 6)

Register	Description
CCR5	Common Control 5
CCR6	Common Control 6

3.2.5 Interrupt on Change of State for RCL, RLOS, RRA, RAIS (section 7)

Register	Description
SR2	Status Register 2
IMR2	Interrupt Mask Register 2

3.2.6 DSO Monitoring (section 9)

Register	Description
CCR5	Common Control 5
CCR6	Common Control 6
TDS0M	Transmit DSO Monitor
RDS0M	Receive DSO Monitor

3.2.7 Hardware Based Signaling (section 10.2)

Register	Description
CCR4	Common Control 4

3.2.8 Per Channel Loopback (section 11)

Register	Description
CCR4	Common Control 4
TIR1-TIR3	Transmit Idle

3.2.9 Per Channel Code Generation (section 11)

Register	Description
TCC1-TCC3	Transmit Channel Control 1-3
TC1-TC24	Transmit Channels 1-24 Codes
RCC1-RCC3	Receive Channel Control 1-3
RC1-RC24	Receive Channels 1-24 Codes

3.2.10 On Chip HDLC & BOC Controller For FDL Support (section 15.1)

Register	Description
TCR1	Transmit Control Register 1
FDLC	FDL Control
FDLS	FDL Status
FIMR	FDL Interrupt Mask
RPRM	Receive Performance Report Message
RBOC	Receive Bit Oriented Message
RFFR	Receive FDL FIFO
TPRM	Transmit Performance Report Message
TBOC	Transmit Bit Oriented Code
TFFR	Transmit FDL FIFO
RDC1	Receive HDLC DS0 Control Register 1
RDC2	Receive HDLC DS0 Control Register 2
TDC1	Transmit HDLC DS0 Control Register 1
TDC2	Transmit HDLC DS0 Control Register 2

3.2.11 Programmable In-Band Code Generation & Detection (section 16)

Register	Description
CCR3	Common Control 3
IBCC	In-Band Code Control
TCD	Transmit Code Definition
RUPCD	Receive Up Code Definition
RDNCD	Receive Down Code Definition
SR1	Status Register 1

3.2.12 Interleave Bus Operation (section 18)

Register	Description
IBO	Interleave Bus Operation Register

3.3 Bit Assignment Changes within Existing Registers

Highlights bit locations in the DS21Q42 which have changed from the DS21Q41B.

Register	Bit #	DS21Q42 Function	DS21Q41B Function
CCR3	0	TESMDM	Not Assigned
CCR3	1	TLOOP	TLU
CCR3	2	ECUS	TLD
CCR3	6	TCLKSRC	ESR
CCR3	7	RESMDM	ESMDM
SR2	0	RSC	LORC
IMR2	0	RSC	LORC

3.4 Register Bit Moves

Register	DS21Q42 Function	DS21Q41B Function
ESR	CCR6 & CCR7	CCR3
LORC	RIR3.4	SR2.0

4.0 Changes in Device Pin Out

4.1 Package types

The DS21Q42 is offered in the same package as the DS21Q41B (128-pin 20 x 20 x 1.4 mm TQFP). Values listed are for body dimensions.

4.2 Device Pin Differences

Pin	DS21Q42	DS21Q41B
9	RSIG0 [RCHCLK0]	RCHCLK0
16	SPARE [RMSYNC0]	RMSYNC0
18	/JTRST\ [RLOS/LOTC0]	RLOS/LOTC0
34	TSIG1 [TCHCLK1]	TCHCLK1
43	RSIG1 [RCHCLK1]	RCHCLK1
46	A7	V _{SS}
47	FMS	V _{DD}
50	JTMS [RMSYNC1]	RMSYNC1
52	JTCLK [RLOS/LOTC1]	RLOS/LOTC1
62	/RD\ / (/DS\)	/RD\ / (/DS\)
68	TSIG2 [TCHCLK2]	TCHCLK2
77	RSIG2 [RCHCLK2]	RCHCLK2
84	JTDI [RMSYNC2]	RMSYNC2
86	JTDO [RLOS/LOTC2]	RLOS/LOTC2
94	TSIG3 [TCHCLK3]	TCHCLK3
103	RSIG3 [RCHCLK3]	RCHCLK3

108	8MCLK [RMSYNC3]	RMSYNC3
112	CLKSI [RLOS/LOT3]	RLOS/LOT3
128	TSIGO [TCHCLK0]	TCHCLK0

NOTE:
Brackets [] indicate pin function when the DS21Q42 is configured for emulation of the DS21Q41B, (FMS = 1).

5.0 Operating the DS21Q42 in DS21Q41B Emulation Mode

The DS21Q42 is a superset of the DS21Q41B and can be configured to emulate the latter. This mode is enabled by tying the Framer Mode Select (FMS) pin to V_{CC} since the DS21Q42 supports an expanded register set, the A7 address pin was added to the device. Although the DS21Q42 does not require the functionality associated with the additional registers when in DS21Q41B emulation mode, the A7 pin must be used. This is necessary because the device does not automatically clear its register space on power-up. After the supplies are stable, each of four framers register space should be configured for operation by writing to all of the internal registers. This can be accomplished in a two-pass approach on each framer.

1. Clear framers register space by writing 00h to the addresses 00h through BFh.
2. Program required registers to achieve desired operating mode.

Application Note 357: <http://www.maxim-ic.com/an357>

More Information

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