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APPLICATION NOTE 336

# Transparent Operation on T1, E1 Framers and Transceivers

*Abstract: The Dallas Semiconductor framers can operate in a transparent mode in both the receive and transmit directions. The transmitter will not insert framing, signaling, or other information such as CRC or FDL. Generally, the receive side of the framers is always transparent. Data received at RTIP and RRING is passed through intact to RSER. All configurations are with the elastic stores disabled. The elastic stores will not alter data except during slip conditions or if configured for 1.544MHz/2.048MHz conversion or signaling reinsertion.*

## Introduction

This application note applies to the following products.

T1 Framers	E1 Framers	T1/E1/J1 Framers	T1 SCTs	E1 SCTs	T1/E1 SCTs
DS21Q41	DS21Q43	DS26401	DS2151	DS2153	DS2155
DS21Q42	DS21Q44		DS2152	DS2154	DS21Q55
DS21FF42	DS21FF44		DS21352	DS21354	DS2156
DS21FT42	DS21FT44		DS21552	DS21554	DS21455
			DS21Q352	DS21Q354	DS21458
			DS21Q552	DS21Q554	DS26521
				DS2150	DS26524
				DS21Q50	DS26528

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## Transparent Operation on DS21Q42, DS21FF42, DS21FT42, DS21352, DS21552, DS21Q352, DS21Q552

Register Configurations:

- TCR1.2, TCR1.5, TCR1.6 = 1
- TCR1.0, TCR1.1, TCR1.4 = 0
- TCR2.0 = 0
- TIR1, TIR2, TIR3 = 00h
- TCC1, TCC2, TCC3 = 00h
- RCC1, RCC2, RCC3 = 00h
- TDC1.7 = 0
- CCR1.5 = 0

RMR1, RMR2, RMR3 = 00h

## Transparent Operation on DS21Q44, DS21FF44, DS21FT44, DS21354, DS21554, DS21Q354, DS21Q554

Register Configurations:

TCR1.6 = 1  
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0  
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0  
CCR1.4 = 0  
CCR2.3, CCR2.4, CCR2.5 = 0  
TIR1, TIR2, TIR3, TIR4 = 00h  
TCC1, TCC2, TCC3, TCC4 = 00h  
RCC1, RCC2, RCC3, RCC4 = 00h  
TSaCR = 00h  
TDC1.7 = 0

## Transparent Operation on DS2152

Register Configurations:

TCR1.2, TCR1.5, TCR1.6 = 1  
TCR1.0, TCR1.1, TCR1.4 = 0  
TCR2.0 = 0  
TIR1, TIR2, TIR3 = 00h  
TCC1, TCC2, TCC3 = 00h  
RCC1, RCC2, RCC3 = 00h  
CCR1.5 = 0  
RMR1, RMR2, RMR3 = 00h

## Transparent Operation on DS2154

Register Configurations:

TCR1.6 = 1  
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0  
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0  
CCR1.4 = 0  
CCR2.3, CCR2.4, CCR2.5 = 0  
CCR4.5 = 0  
TIR1, TIR2, TIR3, TIR4 = 00h  
TCC1, TCC2, TCC3, TCC4 = 00h  
RCC1, RCC2, RCC3, RCC4 = 00h

## Transparent Operation on DS2155, DS2156, DS21455, DS21458 and DS21Q55 for E1 Mode

Register Configurations:

MSTRREG = 02h  
T1RCR1= 00h, T1RCR2= 00h

T1TCR1= 00h, T1TCR2= 00h  
T1CCR1 = 00h  
E1RCR1 = 00h, E1RCR2 = 00h  
E1TCR1= 80h, E1TCR2= 00h  
CCR1 = 00h, CCR2 = 00h, CCR3 = 00h, CCR4 = 00h  
H1TC = 00h, H2TC = 00h

## Transparent Operation on DS2155, DS2156, DS21455, DS21458 and DS21Q55 for T1 Mode

Register Configurations:

MSTRREG = 00h  
T1RCR1= 1Eh, T1RCR2= 60h  
T1TCR1= 60h, T1TCR2= 80h  
T1CCR1 = 04h  
E1RCR1 = 00h, E1RCR2 = 00h  
E1TCR1= 00h, E1TCR2= 00h  
CCR1 = 00h, CCR2 = 00h, CCR3 = 00h, CCR4 = 00h  
H1TC = 00h, H2TC = 00h

## Transparent Operation on DS21Q50 for E1 Mode

Register Configurations:

RCR1 = 00h  
CCR1 = 00h, CCR2 = 00h, CCR3 = 00h, CCR4 = 00h  
CCR5 = 00h  
TIR1 = 00h, TIR2 = 00h, TIR3 = 00h, TIR4 = 00h

## Transparent Operation on DS2151, DS21Q41

Hardware Considerations:

TSER and TLINK must be tied together either logically or physically.

Register Configurations:

TCR1.2, TCR1.5, TCR1.6 = 1  
TCR1.0, TCR1.1, TCR1.4 = 0  
TCR2.0 = 0  
TIR1, TIR2, TIR3 = 00h  
CCR1.5 = 0  
RMR1, RMR2, RMR3 = 00h

## Transparent Operation on DS2153, DS21Q43

Hardware Considerations:

Need rev A5 or better for complete receive transparency with elastic store enabled (DS2153 only).

Register Configurations:

TCR1.6 = 1  
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0  
CCR1.4 = 0  
CCR2.3, CCR2.4, CCR2.5 = 0  
TIR1, TIR2, TIR3, TIR4 = 00h  
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0  
RCR2.1 = 0 (required on rev A2 devices only)

In order to get transparent mode working on the devices DS26401, DS26521, DS26524 and DS26528, the customer should never set the RMMR and TMMR INIT\_DONE bits to 1. Doing so will cause the framer to search for the framing pattern.

## Transparent Operation on DS26401 for E1 Mode

Register Configurations:

RMMR = 81h  
RCR1 = 22h, RCR2 = 00h  
TMMR = 81h  
TCR1= 80h, TCR2= 00h

## Transparent Operation on DS26401 for T1 Mode

Register Configurations:

RMMR = 80h  
RCR1= CAh, RCR2= 0Ch  
TMMR = 80h  
TCR1= 64h, TCR2= 00h, TCR3= 00h

## Transparent Operation on DS26521, DS26524 and DS26528 for E1 Mode

Register Configurations:

RMMR = 81h  
E1RCR1 = 22h, E1RCR2 = 00h, E1RCR3 = 00h  
TMMR = 81h  
E1TCR1= 80h, E1TCR2= 00h, TCR3 = 00h

## Transparent Operation on DS26521, DS26524 and DS26528 for T1 Mode

Register Configurations:

RMMR = 80h  
T1RCR1= CAh, T1RCR2= 0Ch  
TMMR = 80h  
T1TCR1= 64h, T1TCR2= 00h, TCR3= 00h

## Conclusion

If you have further questions about transparent operation on Dallas Semiconductor framers or SCTs, contact the

Application Note 336: <http://www.maxim-ic.com/an336>

### More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

Other questions and comments: <http://www.maxim-ic.com/contact>

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DS21354: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS2152: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS2154: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

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DS21FF42: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

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