

APPLICATION NOTE 3227

Power-On Reset and Related Supervisory Functions

Abstract: This article describes both the function of power-on resets and the strategies for choosing their threshold voltages, when used with single-supply and dual-supply processors. It then discusses manual reset and power-fail and low-line signals. The article demonstrates why to avoid discrete PORs and PORs internal to processors. It concludes with explanations of voltage sequencing, voltage tracking, and reset sequencing.

One task of the power-on reset (POR) is ensuring that the processor starts at a known address when power is first applied. To accomplish that task, the POR logic output holds the processor in its reset state when the processor's power supply is first turned on. The POR's second task is to keep the processor from starting its operation from that known address until three events have occurred: the system power supplies have stabilized at the appropriate levels; the processor's clock(s) has (have) settled; and the internal registers have been properly loaded. The POR accomplishes this second task through an onboard timer, which continues to hold the processor in its reset state for a prescribed period of time. That timer triggers after the processor's power supply reaches a specific voltage threshold. After a set time elapses, the timer expires, causing the POR output to become inactive, which in turn makes the processor come out of reset and begin operation (**Figure 1**). The processor's data sheet specifies the required duration of the timer's delay. The timer, incidentally, is what differentiates a POR from a voltage detector, a device that also detects a voltage threshold, but does not time an event.

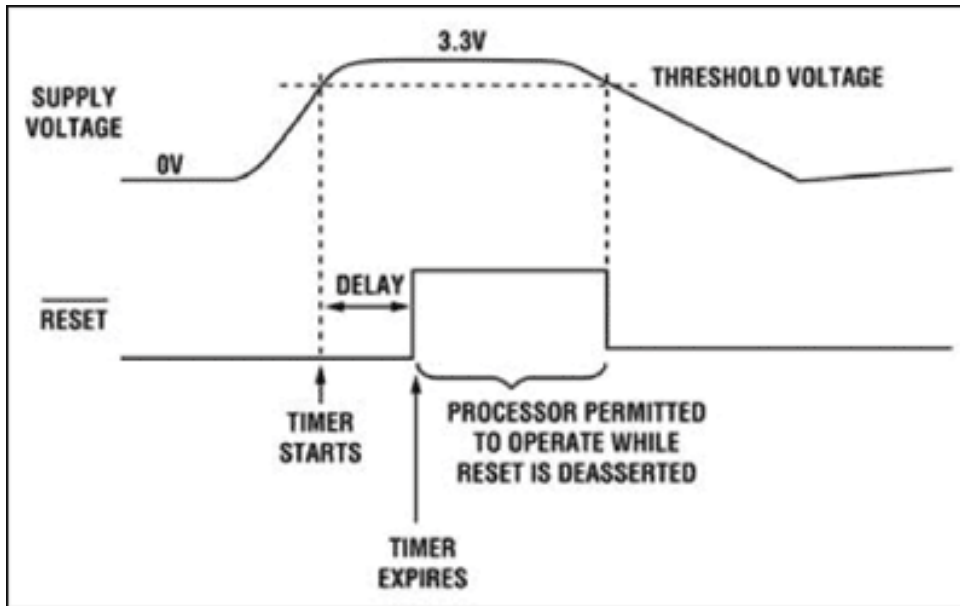


Figure 1. A POR holds a processor in its reset state until the supply voltage exceeds the POR threshold and a specific delay period has elapsed.

The superior noise immunity of a POR, which is necessary when monitoring a processor, also distinguishes it from a voltage detector. This is because a POR should not issue a reset when a small, fast glitch appears on the supply, as the processor itself does not react to such glitches. However, both a small glitch of long duration and a large glitch of short or long duration can cause problems for the processor. Therefore, the best approach is to use a POR that examines both the size and duration of disturbances to the power-supply voltage for determining when to assert a reset. The intent is to mirror the processor's own behavior and to assert a reset only when one is needed, as there is no point in resetting the processor if it is working properly. **Figure 2** is a graph from the MAX6381/MAX6382 data sheet that details an example of the magnitude/duration of the supply-voltage disturbance required to trigger a reset. This graph illustrates that the MAX6381/MAX6382 issues a reset when the monitored power supply is 100mV below the specified threshold for at least 10ms.

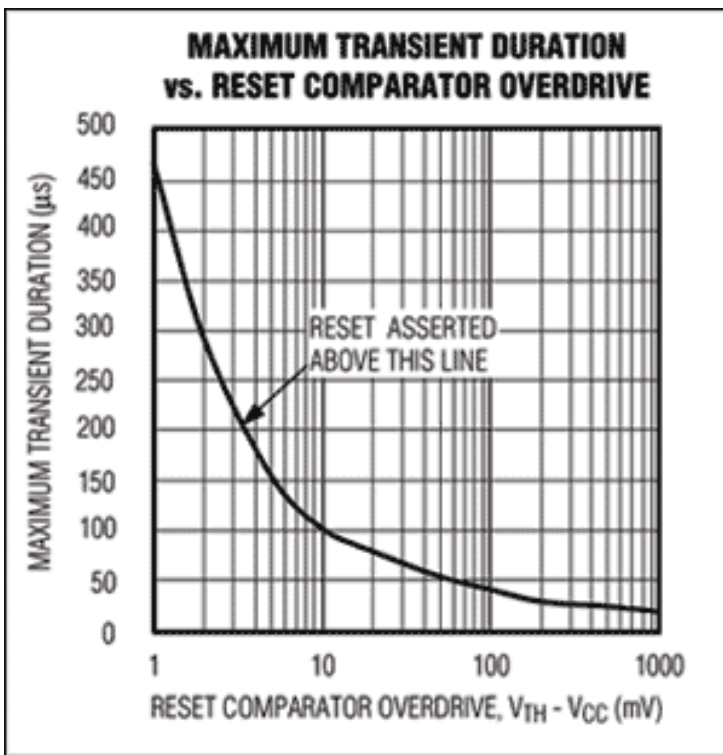


Figure 2. Whether a POR generates a reset is a function of both the amplitude and duration of the glitch.

Should the supply voltage return above the threshold, the POR timer allows the reset signal to deassert only after the prescribed interval.

Some processors provide a bidirectional reset pin—a pin that can not only receive a reset signal, but can also transmit one. At first glance, a POR with an open-drain output would seem to be needed in this situation. However, other considerations apply, because the processor must determine whether it or an external device initiated the reset. A POR specially configured for such a situation is necessary (refer to the MAX6314 data sheet).

Determining the POR Threshold Voltage - Single-Supply Processors

Determining the correct POR threshold level and the required accuracy for that level are both often misunderstood. To shed light on those tasks, assume a processor is used that guarantees accurate operation with a $3.3V \pm 0.3V$ supply voltage - specifically, from 3.00V to 3.60V. Board designers follow one of two strategies when choosing the threshold voltage.

One strategy is to ensure that the tolerance of the 3.3V supply is tight enough so they can use a POR with a threshold plus tolerance that remains entirely within the $\pm 0.3V$ range. In that case, the POR threshold lies between the lower end of the supply's range ($\pm 3\%$) and the lower end of the processor's allowed voltage range (**Figure 3a**). Under this strategy, the POR does not issue a reset when the supply is within tolerance. However, the POR does issue a reset when the supply voltage has dropped below its tolerance level, and remains within the range where the processor is guaranteed to operate correctly. This ensures that reset occurs before the processor can operate erroneously at a voltage below its guaranteed operational level.

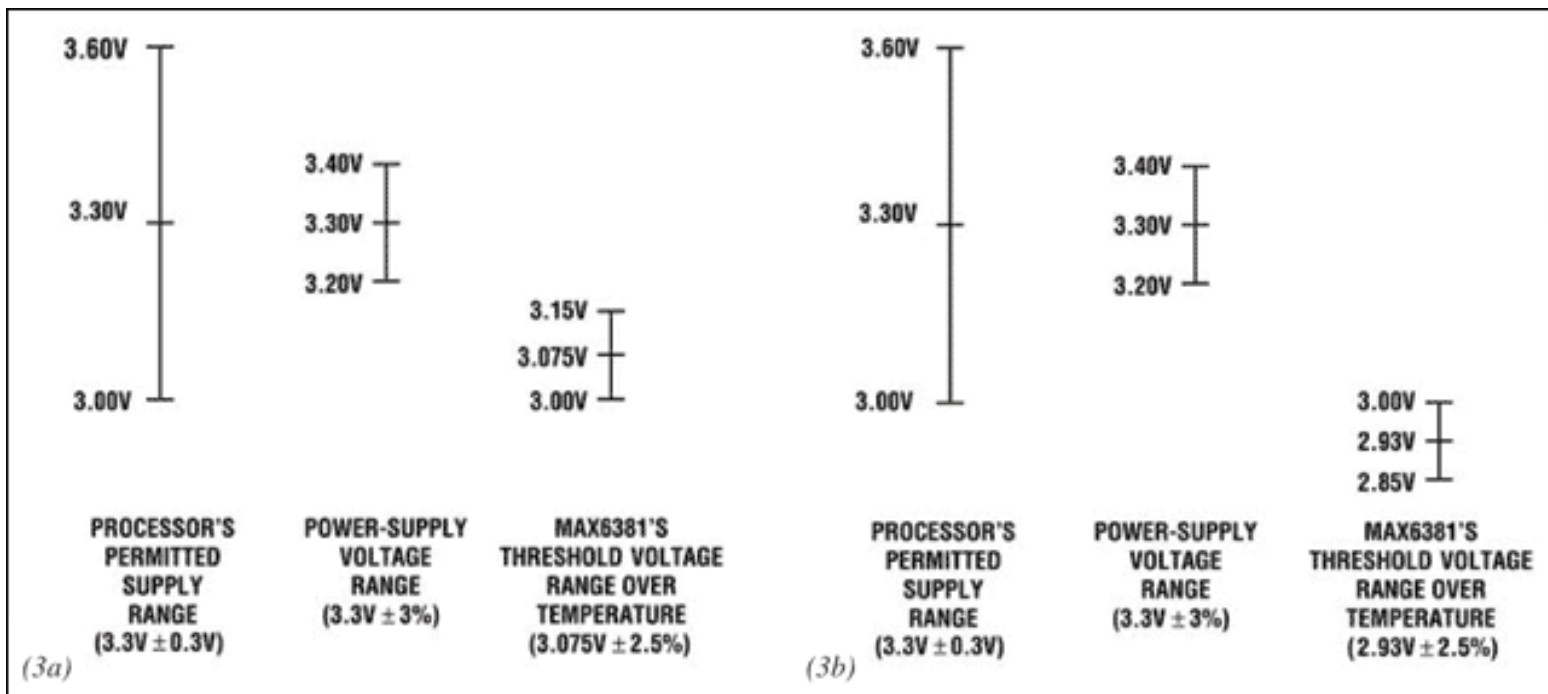


Figure 3. To ensure that the processor gets reset when the supply voltage is below the power supply's specified voltage range and above the bottom of the processor's range of permitted voltages, choose a POR threshold as shown in Figure 3a. However, choosing a POR threshold below the processor's range of permitted voltages (Figure 3b) guarantees that reset will not occur anywhere within that range and allows the use of a power supply with a looser tolerance.

A suitable choice of POR for this strategy is the version of the MAX6381 with a threshold range of 3.00V to 3.15V over temperature (Figure 3a). With this POR included, the processor will reset after the power supply drops below its specified voltage range, but before the supply drops below the processor's specified voltage range. Also, given that the upper end of the threshold's range is 3.15V, a reset cannot occur when the power supply is within its allowed range. However, voltage drops through the edge connector and board trace that connect the supply voltage to the processor might cause the voltage at the processor to drop below 3.15V. In this case, a reset could occur even though the supply voltage is within specifications. A tighter tolerance supply or tighter tolerance POR threshold, or both, would be necessary.

This design approach is more susceptible to power-supply glitches and noise, because the supply voltage can be fairly close to the POR threshold (depending on where the POR threshold and supply voltage lie within their tolerances). Therefore, this approach is appropriate for systems where glitches and noise are minimized and power-supply tolerances are tight.

Some board designers adopt a second, different strategy when choosing a POR threshold level. They employ a POR with a threshold below the processor's guaranteed operating voltage (3.00V, in this example). This allows the processor to operate anywhere within the range of permitted voltages without encountering a reset. It also permits a looser tolerance power supply. These designers are comfortable assuming that, during power-up, the power supply will continue to rise above the POR threshold level and settle within its specified range of voltages (3.20V to 3.40V, in this case). This is expected to happen well before the POR timer times out and the processor begins to operate. Often, designers use the power-OK signal provided by some power supplies to ensure that the supply operates within its specified range.

These same designers are unconcerned about the effect of a brownout condition. If a brownout occurs, the processor could encounter a supply voltage that falls below its minimum guaranteed operating voltage, but remains briefly above the POR threshold level (beneath which the POR would generate a reset). While powered by supply voltages in that range, the processor could operate erroneously.

Contrary to choosing a threshold within the processor's permitted supply voltage range, the second approach is more appropriate for those systems where glitches and noise tend to be larger, because the POR threshold and the power-supply voltage are further apart. As mentioned above, this also permits wider tolerance power supplies.

The version of the MAX6381 that has a threshold range of 2.85V to 3.0V over temperature is a good choice here, because the threshold is below the low end of the processor's permitted range (Figure 3b). One could also use a power supply with a tolerance wider than that shown in Figure 3.

Occasionally board designers position their power supply's nominal voltage closer to the lower end of the processor's permitted range to reduce power consumption. Doing this can be quite effective, because power consumption is proportional to the square of the supply voltage. Given the 3.0V to 3.6V range of permitted processor voltages, a 3.15V ± 2% supply would be suitable, provided there is no significant voltage drop through the edge connector and trace that connects the supply to the processor. The MAX6381 POR with the 2.85V to 3.0V threshold voltage range would be an appropriate choice, if noise levels are sufficiently low to prevent false resets.

Determining the POR Threshold Voltage—Dual-Supply Processors

If a processor requires another supply (e.g., a 1.8V core supply) in addition to a 3.3V supply, then the design may call for a POR that monitors two voltages. This type of POR deasserts its reset only after both supplies are above the POR's two corresponding thresholds and the required timeout period has passed. PORs that monitor two, three, and four voltages are available.

The same choices apply when monitoring multiple supplies or a single supply. For the dual-supply case (e.g., 3.3V and 1.8V), one can elect to use a POR with two thresholds that are both above or below the processor's minimum guaranteed operating voltages. Also, one could use a threshold that is below the guaranteed operating voltage for the 3.3V I/O supply and another threshold that is above the guaranteed operating voltage for the 1.8V core supply. Some board designers opt for the latter strategy, because sometimes the core of the processor is more sensitive than its I/O to problems caused by a low supply voltage.

Core supply voltages have consistently dropped over time, and thus reduced POR threshold voltages have become necessary. Devices within the MAX6736 family provide thresholds as low as 788mV without external resistors, and as low as 488mV with external resistors. These thresholds are low enough to monitor most modern core voltages.

For low-cost systems, some circuit designers elect to monitor only the 3.3V supply if the 1.8V supply is derived from it. They assume that if the 3.3V supply reaches its correct voltage, the 1.8V supply will follow. For systems requiring higher reliability, designers usually decide to monitor both supplies.

Manual Reset

It is often useful to manually trigger a reset while the power-supply voltage remains within tolerance. Not only is this feature used for debugging and final testing, it is also valuable when the processor locks up—it allows the processor to restart without turning off the power. This function is especially useful for those products with processors that are never powered down. It is common for an on/off switch to only wake up/suspend the processor without ever turning off the processor power.

Although a logic signal from an I/O line, a watchdog timer, or a power-fail output often initiates a manual reset, a pushbutton switch can also be used. When pressed, this type of switch usually bounces, opening and closing several times before settling in the appropriate state. Therefore, most manual-reset inputs include debounce circuitry that ignores the ringing caused by the pushbutton switch.

Discrete PORs and PORs Internal to the Processor

Using a discrete POR created with a resistor and capacitor (**Figure 4a**) is a risky proposition. The longer rise and fall times at the output of this type of POR can create problems for some processors—especially those with reset inputs not including a Schmitt trigger and for those with bidirectional reset pins. Adding a Schmitt trigger can help the former case, but can also contribute to cost, space, and startup issues.

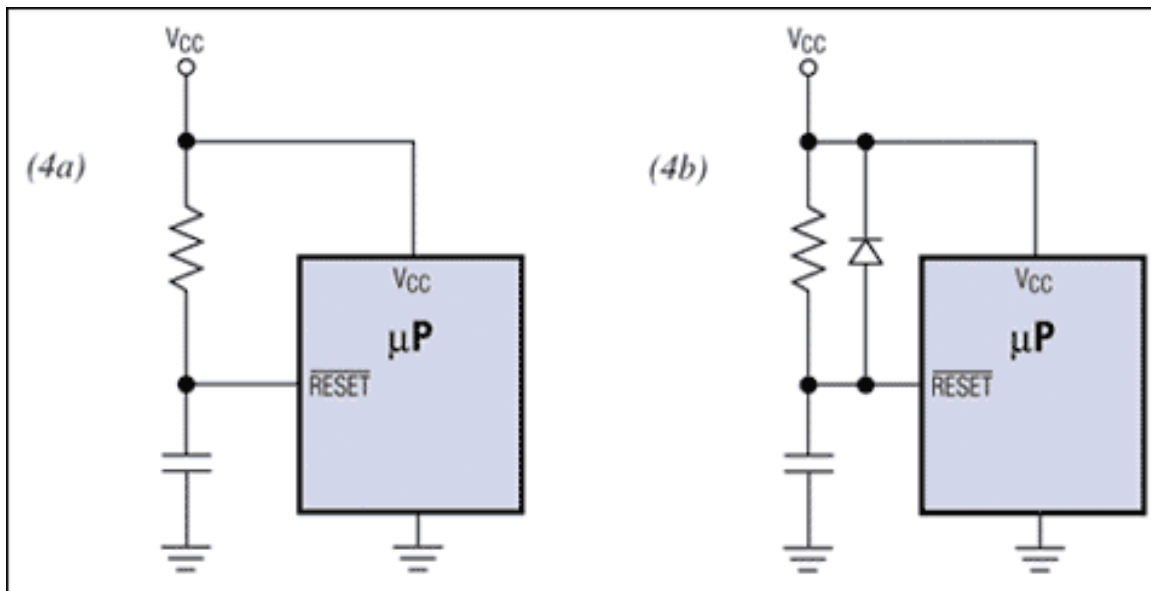


Figure 4. The discrete R/C POR (Figure 4a) is not reliable enough for most applications. In some cases, adding a diode to the circuit (Figure 4b) corrects quick-supply-cycling problems and improves the circuit's performance.

Another problem arises when a discrete POR is used along with a supply that, when powering up, rises slowly in relation to the POR time constant. The processor can come out of reset well before it has stabilized. To prevent this problem, the time constant of the R/C circuit may need to be increased. Also, some manufacturers whose processors include an internal POR, recommend that an R/C (plus a diode described below) be added to the reset input if the power supply comes up slowly.

If the power supply has a glitch after power up, the R/C circuit might filter that glitch, thus preventing a reset from happening. Also, if the supply droops, the voltage at the processor's reset pin could remain higher than its V_{IH} , which is too high for a reset to occur. This can transpire even when the supply has dropped below the processor's minimum guaranteed operating voltage. This happens because a reset pin's V_{IH} is often lower than the processor's minimum guaranteed operating voltage. Another problem can arise if the power is turned off and then on again quickly—the capacitor might not have sufficient time to discharge prior to the power coming back on.

By adding a diode (Figure 4b), the R/C circuit can respond to glitches, because the diode quickly discharges the capacitor whenever a glitch appears. The glitch must be sufficiently large to drop the voltage at the reset pin to V_{IL} (min). Additionally, the other problems listed previously for the R/C circuit without the diode can potentially plague this circuit. However, sometimes the diode does fix the problem created when the supply is quickly cycled off and on.

Using an integrated POR makes the most sense for most equipment, as this device creates none of these problems.

Using a POR internal to a processor can also cause difficulties. These PORs often suffer from inaccuracy and can exhibit problems at lower voltages. Furthermore, some internal PORs are set up to provide a reset during powerup, but not when the supply voltage dips during a brownout condition. Some manufacturers suggest adding a discrete circuit to accommodate that condition.

Finally, a system powered by multiple supplies may pose another problem for an internal POR. For example, you could encounter a problem when an internal POR timeout period is appropriate for its processor, but not for external circuitry (e.g., memory) whose supply voltage comes up more slowly. In that case, a solution would be an external POR with a longer delay time that monitors both the processor and the external-circuit supplies.

Power-Fail and Low-Line Signals

Supervisor circuits that include power-fail or low-line signals warn the processor that a brownout or power failure is imminent. When either of those signals interrupts the processor, the processor can enter a power-down routine. This routine causes the processor to cease its current activities and back up important data prior to the POR placing the processor in reset.

To create a power-fail signal, the supervisor's power-fail comparator monitors the unregulated DC voltage (or some other upstream regulated voltage). This voltage feeds the regulator, which powers both the processor and supervisor circuit. The unregulated voltage drops before the regulator's voltage because the regulator's output capacitor retains its output voltage (**Figure 5**). Thus, a drop in the unregulated voltage indicates a possible drop in the regulator's voltage. Detecting that drop and interrupting the processor allow the processor to enter its power-down routine prior to being reset, if the powersupply voltage were to drop low enough.

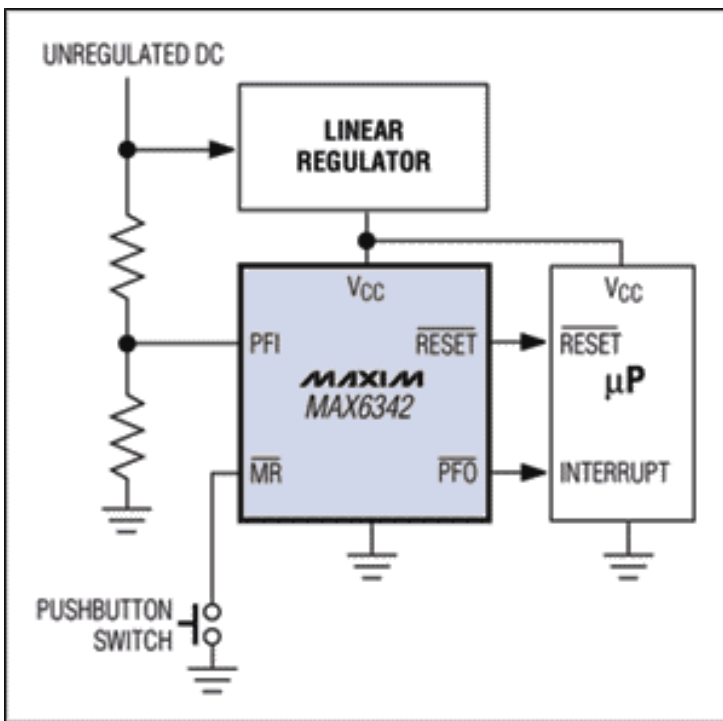


Figure 5. The power-fail comparator within the MAX6342 generates the power-fail signal (PFO-bar) by monitoring whether the unregulated DC supply has dropped.

When there is no access to the unregulated voltage (or an upstream regulated voltage), the processor can still receive warning of an imminent power failure. That warning could come from a supervisor that provides a low-line signal, which goes active whenever the monitored power supply drops to a level slightly above the reset threshold (e.g., 150mV above). Thus, the low-line signal warns the processor that the power-supply voltage may decrease enough to cause the POR to issue a reset. Here, as with a power-fail comparator's signal, the processor backs up important data in anticipation of the POR generating a reset due to a brownout or power failure.

Voltage Sequencing and Voltage Tracking

Most data sheets of processors powered by two supplies specify the order in which the supplies should come up. Parts such as the MAX6819/MAX6820 can sequence the supplies in the proper order. If the processor's supplies are not sequenced properly, the processor can latch up, initiate incorrectly, or endure long-term reliability degradation. Sometimes, the various supply voltages are not locally generated (e.g., they come from a main system bus, an externally purchased silver box, or supplies that do not include enable and power-OK pins that facilitate sequencing). In such cases, power-on and power-off sequencing can be difficult to control or predict, thus making a voltage-sequencing IC necessary. This type of IC is also needed when different resistive and capacitive loads affect the turn-on and turn-off times of the various supplies. This makes it difficult to predict the order in which the supplies power up and down.

A unique method for sequencing two power supplies is found in the MAX6741/MAX6744. These devices work by first allowing one supply to power up. Then, after a delay period, they allow the second power supply to power up by issuing a power-OK signal, which takes the supply out of shutdown. After both supplies are up and another time delay elapses, the MAX6741/MAX6744 reset signal deasserts.

Some processors require that the two supplies track each other during power up. In that case, the MAX5039/MAX5040 can achieve tracking by clamping the two supplies together until the lower-voltage supply reaches its final voltage. At this point, the higher-voltage supply is free to continue up to its final voltage.

Reset Sequencing

When a circuit incorporates two processors, often one processor must come out of reset prior to the second. Previously, board designers wired two PORs together to handle this requirement. The output of the first POR both reset the first processor and controlled the manual-reset input of the second. The second POR output reset the second processor (or, in some cases, the memory). Currently, dual PORs with time-staggered reset outputs are available for this task (Figure 6). These PORs assert both reset outputs whenever the master supply voltage (3.3V, in Figure 6) strays below the POR's internally set threshold. (The slave POR asserts slightly before the master.) Once the supply returns above this threshold, one of the two reset outputs deasserts after its timer has timed out (active-low RESET1, in Figure 6). For the second POR to initiate its timer and deassert its output, two conditions must be met: active-low RESET must be deasserted; and the slave

supply voltage, monitored by the second POR, must be above the threshold set by external resistors. If the same supply voltage powers both processors, RSTIN2 can be connected directly to the supply instead of using a voltage divider.

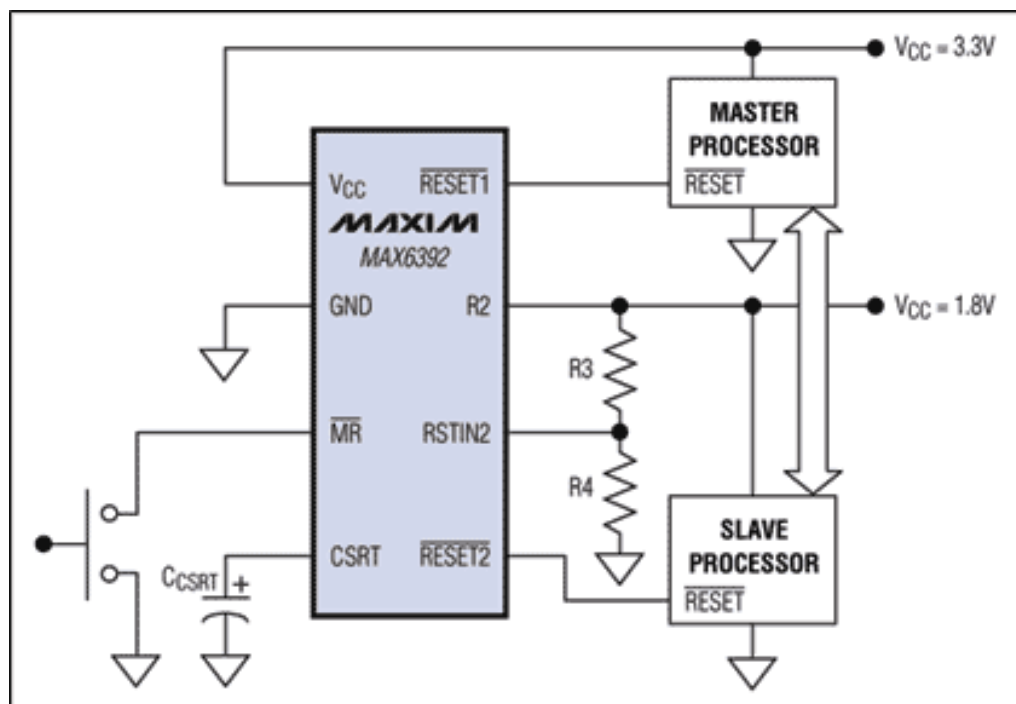


Figure 6. This circuit allows the master processor to come out of reset prior to the slave by monitoring the supplies that power the two processors.

For the MAX6392 shown in Figure 6, the second POR output always comes out of reset after the first output. In fact, the time specified for it to come out of reset is measured from the time that the first output deasserts. Thus, the Figure 6 circuit forces the slave processor to come out of reset after the master processor has begun operating. The second POR delay time can be increased by adding a capacitor to the IC.

If three processors need to be sequenced, the DS1830 can be considered. The three PORs within this device operate with minimum reset periods of 10ms, 50ms, and 100ms from the time the power-supply voltage crosses the POR threshold. A single logic pin allows multiplication of those reset periods by a factor of two or five.

Conclusion

Although choosing the appropriate microprocessor supervisor and operating it correctly are often straightforward, some aspects of that exercise may require careful planning. Such is the case with power-on resets. Choosing the correct voltage and tolerance for both the power supply and the POR threshold requires some thought. Also, well worth considering are newer devices that accommodate processor requirements such as multivoltage reset, reset sequencing, power sequencing, and voltage tracking.

A similar article appeared in the April, 2004 issue of *EDN*.

Application Note 3227: <http://www.maxim-ic.com/an3227>

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