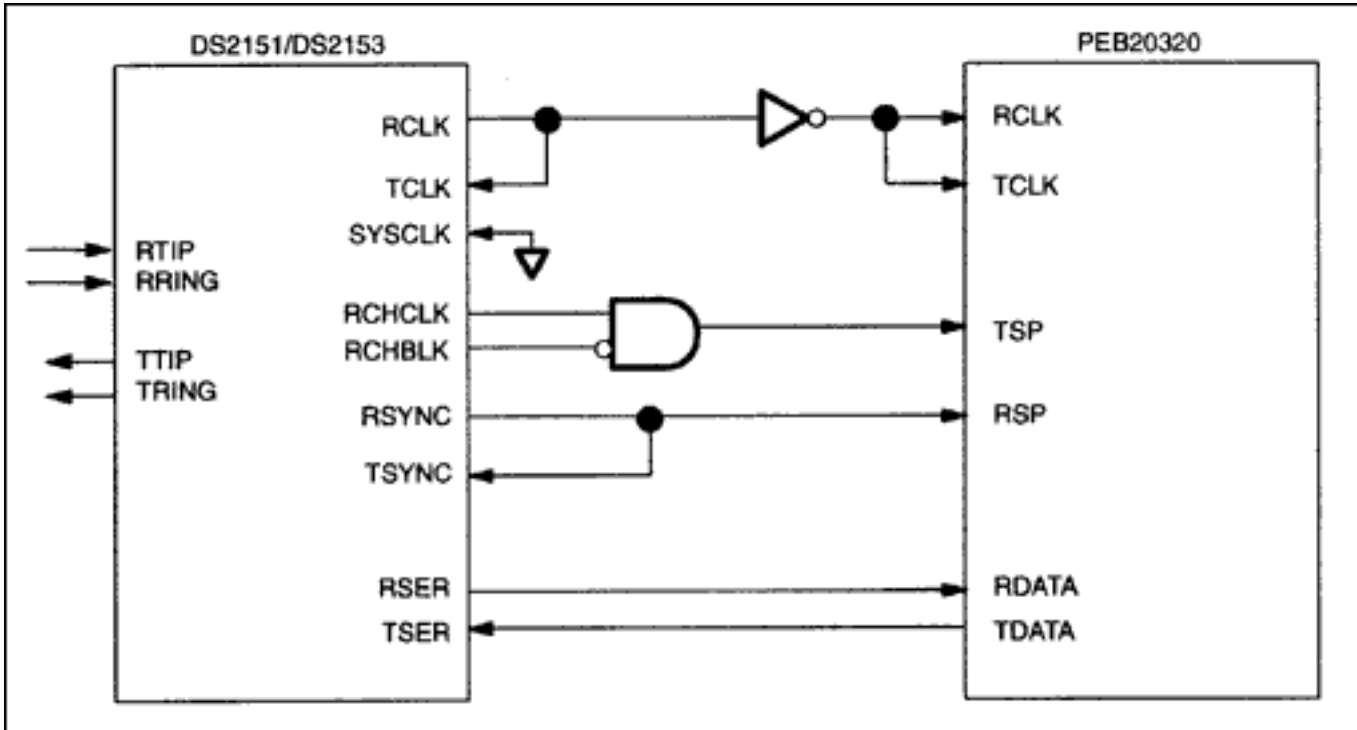


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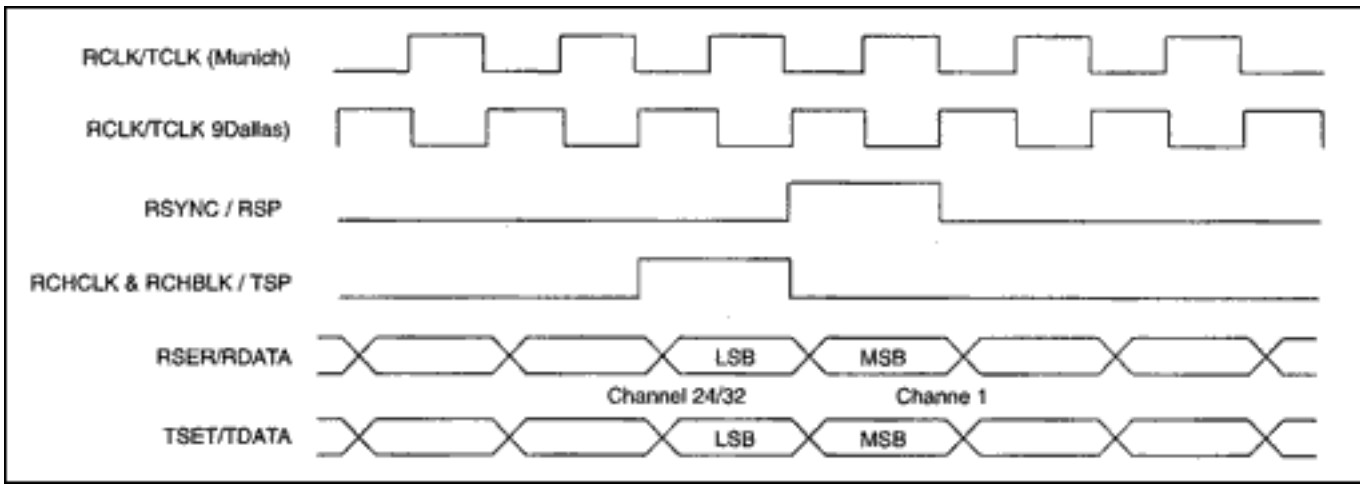
## DS2151, DS2153 Interfacing to the PEB20320

*Abstract: Application Note 312 provides a logical diagram of the interface of the Dallas Semiconductor/Maxim DS2151 T1 single chip transceiver (SCT) and DS2153 E1 SCT to the Siemens PEB20320.*



### Notes:

1. Both the DS2151 and the DS2153 are set up with both the receive and transmit elastic stores disabled.
2. Shown is a "looped-timed" application.
3. The RSYNC pin is programmed to be an output; the TSYNC pin is programmed to be an input.
4. RCHBLK is programmed to be set high except in the last channel of each frame.
5. Timing between the devices is shown below:



Application Note 312: <http://www.maxim-ic.com/an312>

### More Information

For technical questions and support: <http://www.maxim-ic.com/support>

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