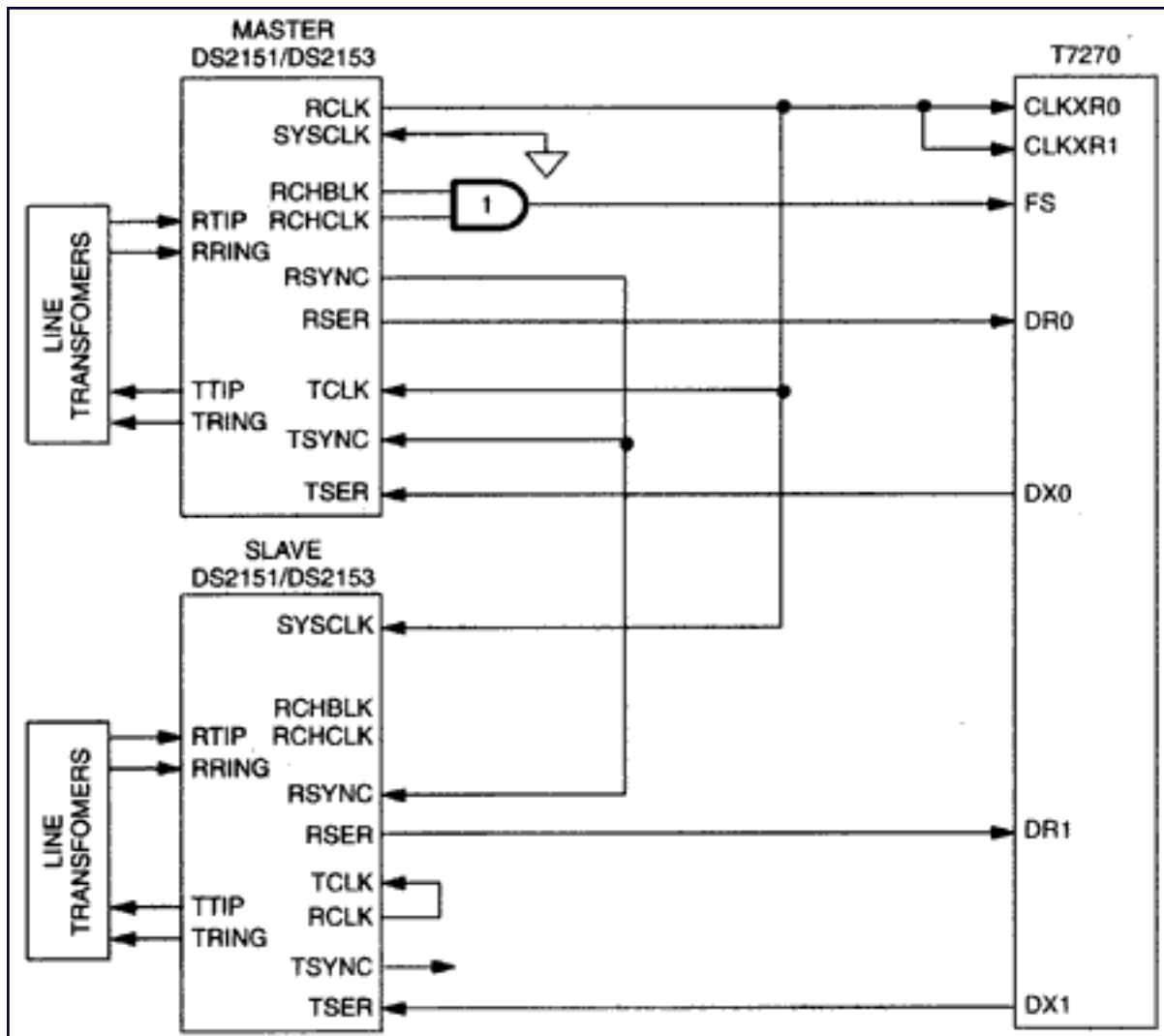


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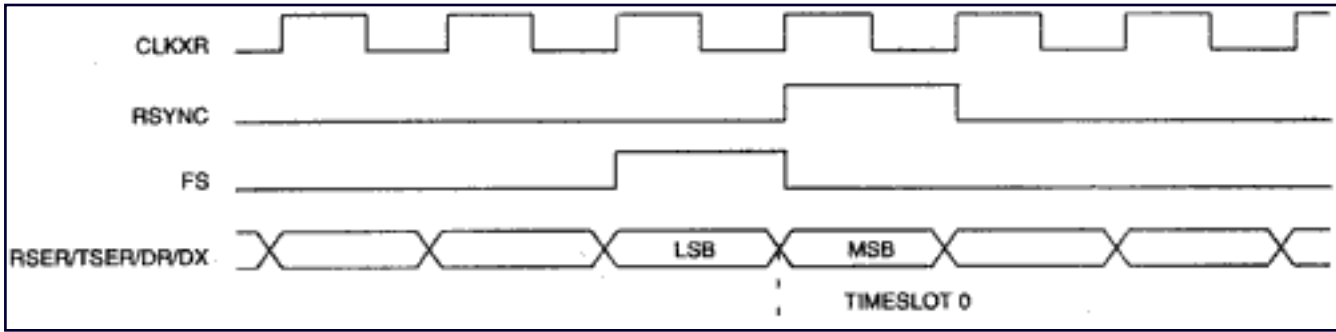
## DS2151, DS2153 Interfacing to the AT&T T7270

Abstract: Application Note 304 provides a logical diagram of the interface of the Dallas Semiconductor/Maxim DS2151 T1 single chip transceiver (SCT) and DS2153 E1 SCT to the AT&T T7270.



### Notes:

1. CMS = 0 in the T7270.
2. Gate #1 is used to condition the frame sync to meet the timing requirements of the T7270.
3. In the master, no elastic stores are enabled; in the slave, both the receive and the transmit side elastic stores are enabled.
4. A "loop-timed" application is shown.
5. In the master, RCHBLK is programmed to go high during the last channel.
6. Timing is shown below:



Application Note 304: <http://www.maxim-ic.com/an304>

### More Information

For technical questions and support: <http://www.maxim-ic.com/support>

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