



APPLICATION NOTE 1879

# Using Maxim SPI-compatible Display Drivers with other SPI Peripherals

*Abstract: This application note discusses techniques to connect Maxim's daisy-chained SPI™-compatible display drivers and GPIO to 3-state SPI devices.*

This application note discusses techniques to connect Maxim's SPI™-compatible display drivers to other SPI devices on a common SPI interface. The discussion applies to the MAX6950, MAX6951, MAX6952, MAX6954, MAX6957, and MAX7221 LED drivers, the MAX6850, and MAX6852 vacuum fluorescent display (VFD) controllers, and the MAX7301 general purpose I/O (GPIO) peripheral.

Motorola's serial peripheral interface (SPI) is a flexible synchronous serial interface superset standard. When implemented within a Motorola microcontroller such as one of the M68HC11 family, the SPI serial interface can be configured to send and receive data with a wide degree of flexibility of polarity and timing of the control signals. The operation of the microcontroller's serial interface is specified by configuration register. These register bits set clock polarity (CPOL) and clock phase (CPHA) as well as speed and detail timings for the serial transmissions. **Table 1** shows the Maxim and Motorola nomenclature for the SPI interface functions.

**Table 1. SPI Interface Connection to a Motorola Microcontroller**

Maxim Pin Name	Maxim Pin Function	Connect to Motorola Pin Name	Motorola Pin Function	Implementation
DIN	Slave Data Input	MOSI	Master Output/ Slave Input	ECH transmission is 16-bits
DOUT	Slave Data Output	MISO	Slave Output/ Master Input	Expected to be a 3-state output
CS	Chip Select Input	SS	Slave Select Output	Set CPHA = 1 (chip/slave select line does not rise at end of each transmitted byte)
CLK	Master Clock Input	SCK	Clock Output	Set CPOL = 0 (slave samples data from master on rising edge of clock)

One issue that may arise is that the Motorola SPI protocol expects all slave devices to use 3-state MISO/DOUT outputs. This architecture allows multiple slaves to be connected to a common MISO/DOUT microcontroller input, and only an addressed slave drives the MISO/DOUT line at any time. The Maxim DOUT pin is, however, not 3-state. The reason for this was that multiple devices were expected to be daisy-chained (cascaded) together by connecting the DOUT of one device to the DIN of the next, and the CLK and CS lines of all devices being driven in parallel. This architecture reduces microcontroller pin count when large numbers of devices are being driven on one serial bus, because only one CS line is required. Since the DOUT of each device is likely to drive the DIN pin of another, the DOUT output remains active. If the DOUT output went high-impedance, the DIN input of a subsequent daisy-chained device would be high-impedance also. The difference between the behaviors is shown in **Figures 1** and **2**.

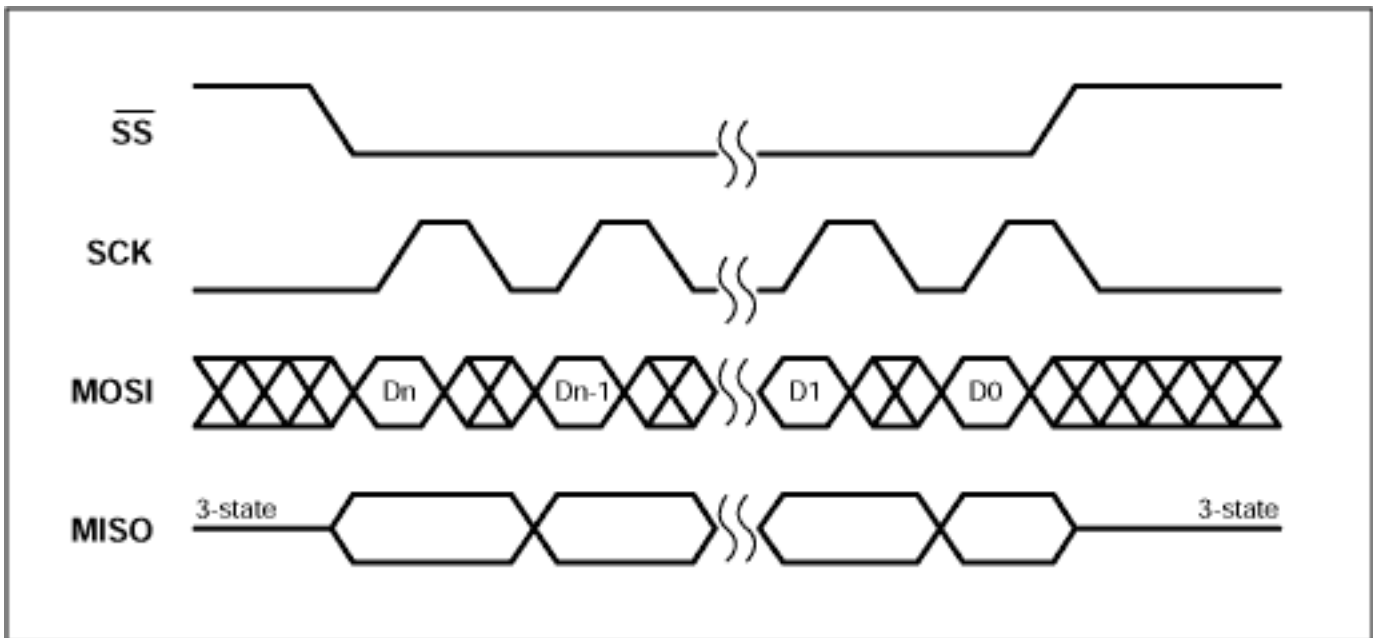


Figure 1. Motorola SPI interface timing (CPHA=1, CPOL=0).

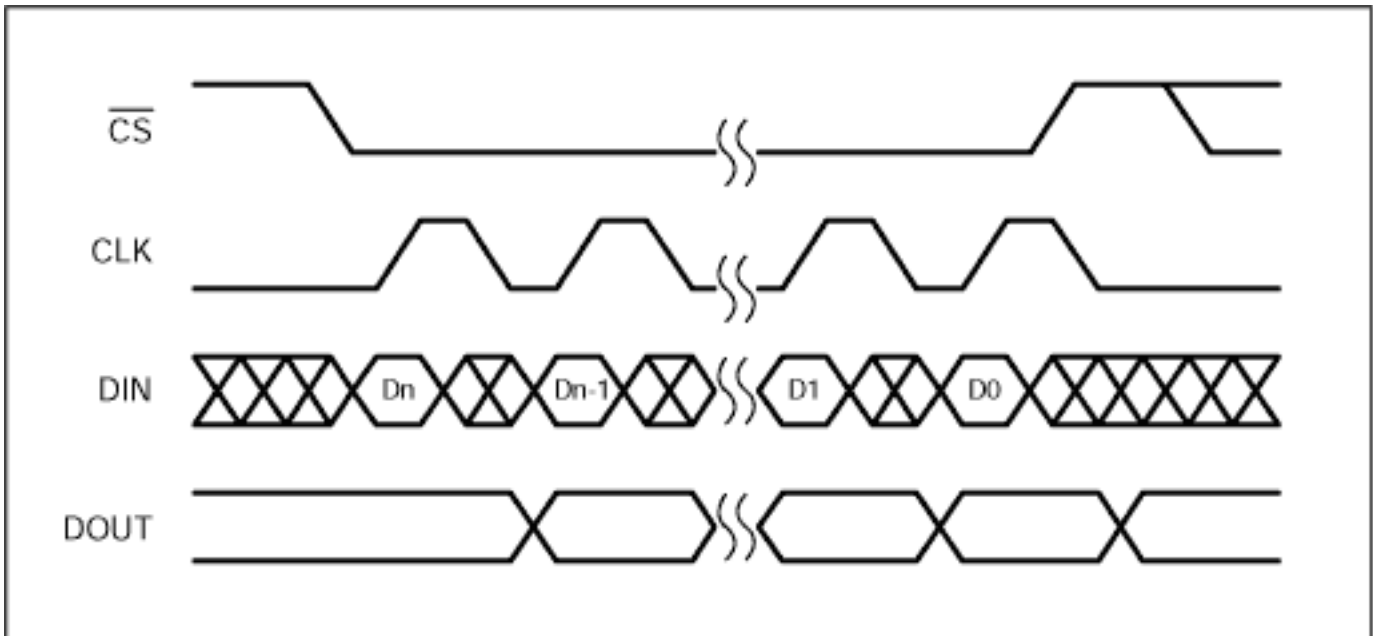


Figure 2. Maxim SPI-compatible interface timing.

If the application demands that a mix of 3-state and non 3-state devices are mixed on the same SPI bus, the non 3-state devices can be converted to 3-state by adding an analog switch or a 3-state buffer between the DOUT pin and the SPI MISO pin (**Figure 3**). The analog switch or a 3-state buffer is gated on when CS goes low, selecting the device and enabling the DOUT at the same time.

Suitable single analog switches are the pin compatible MAX4595 and MAX4502 in small SC-70 and SOT-23 packages (**Figure 4**). Alternatively, one third of a MAX4053 or 74HC4053 triple SPDT switch could be used. Suitable single 3-state buffers are the pin compatible Fairchild TinyLogic NC7SZ125 and TI SN74AHC1G125. The standard 74HC125 contains 4 such 3-state buffers in a single package.

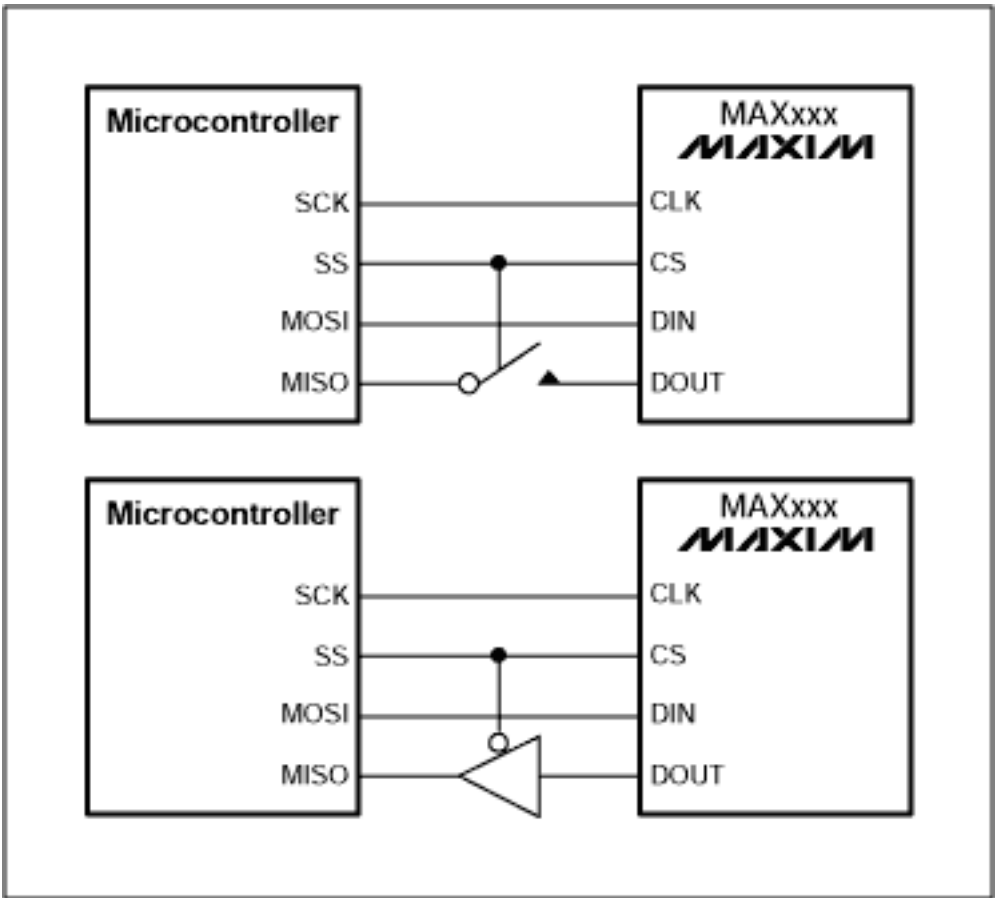


Figure 3. Using an analog switch or 3-state buffer to create a 3-state DOUT.

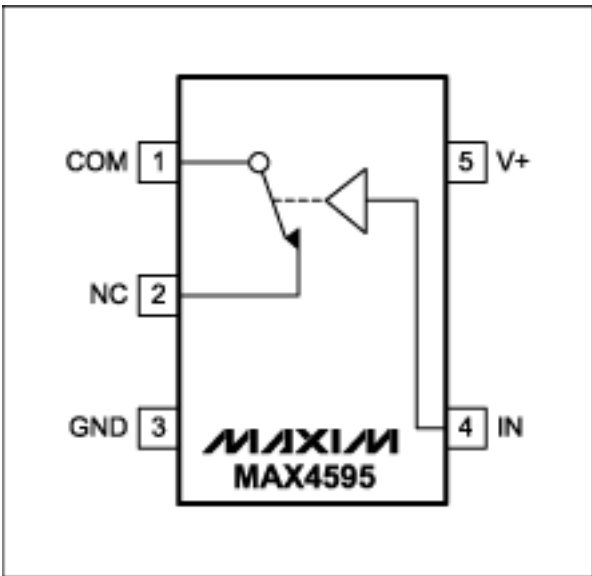


Figure 4. MAX4595 and MAX4502 SPST analog switch pinout.

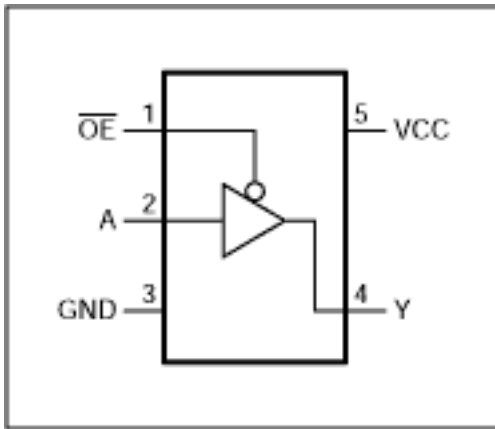


Figure 5. NC7SZ125 and SN74AHC1G125 pinout.

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