

APPLICATION NOTE 1779

Tech Brief 40: Understanding Programmable Delay Lines: Overview of the DS1020, DS1021, DS1023, and DS1045

Abstract: This is an earlier application note discussing the characteristics and capabilities of the DS1020, DS1021, and DS1045 programmable delay lines from Dallas Semiconductor. It discusses the architecture and functionality of the two programmable delay line families: The single delay DS1020/DS1021/DS1023 and the dual delay line DS1045. Delay characteristics required by the design engineer such as linearity and effects of temperature are also discussed.

Introduction

The system timing and control family includes programmable delay lines. These devices offer the user the ability to program the required delay after installation in the application rather than use factory-trimmed fixed-delay intervals. Economic considerations usually dictate that this approach is used whenever dynamic delay adjustment is needed in the system, rather than as a convenience to avoid specifying particular fixed delay values.

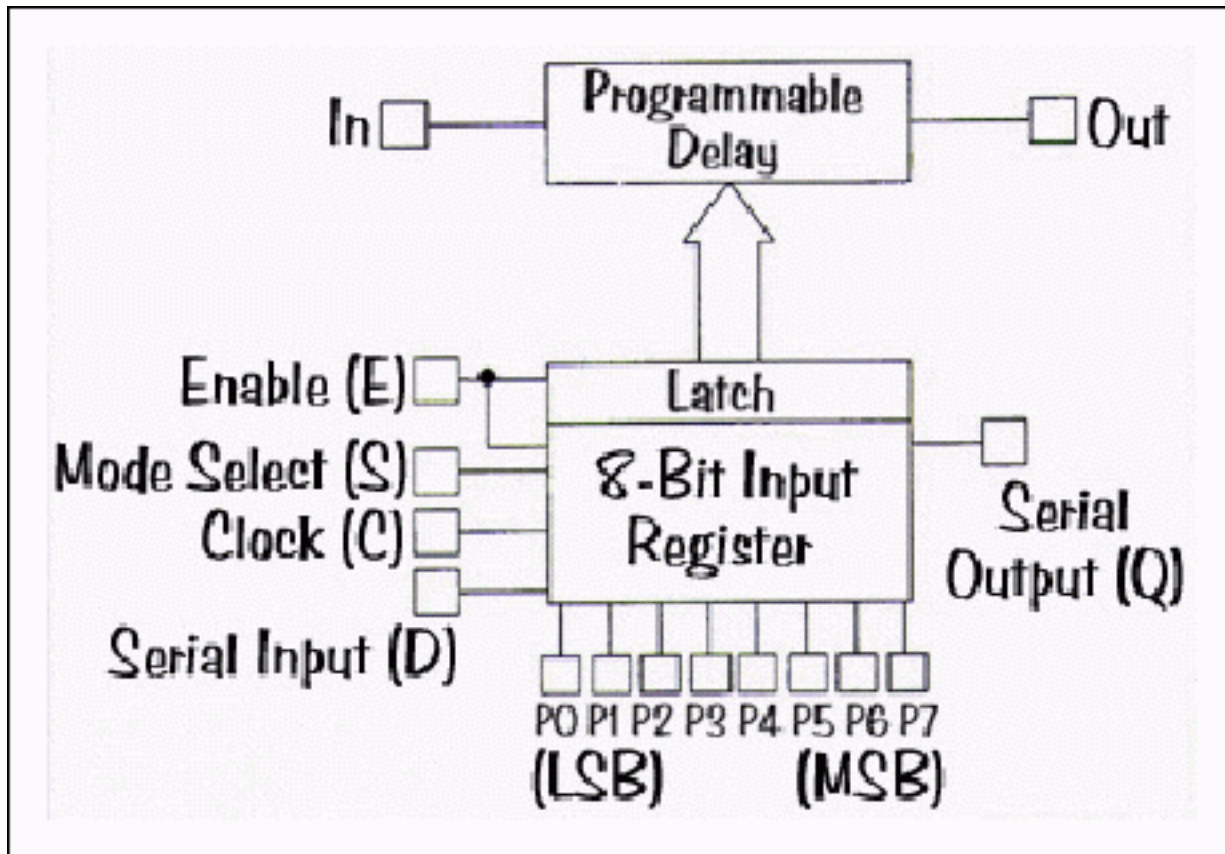


Figure 1.

DS1020/DS1021/DS1023 8-Bit Programmable Silicon Delay Lines

These devices can be used in many of the same configurations illustrated here when dynamic alteration of system parameters is needed. The DS1020, DS1021, and DS1023 offer both parallel and serial methods of programming. In the parallel mode, an eight-bit word applied directly to a multiplexer, which selects the delay time desired. These values may also be set via a three-wire serial bus.

The DS1020 is a single 8-bit programmable delay line with a choice of serial or parallel programming. Step sizes of 0.15ns, 0.25ns, 0.5ns, 1ns, and 2ns are available. The DS1021 is a similar, but lower-cost, device. It is offered only in SO packaging, with step sizes of 0.25ns or 0.5ns only. The DS1023 is a more fully-featured device than the DS1020 and DS1021. It has an inherent step zero delay time of 16.5ns, with steps sizes of 0.25ns, 0.5ns, 1ns, 2ns, and 5ns. In addition to the standard features, it includes a step-one reference delay output, a pulse-width modulator output option, and an inverted output option. It is constructed using a different topology that allows delay times greater than the pulse width.

DS1045 4-Bit Dual Programmable Delay Line

The DS1045 is effectively a 4-bit programmable delay line with two simultaneous programmable outputs from a single input. This device is particularly useful for skew adjustments as it allows either output to lead or lag the other.

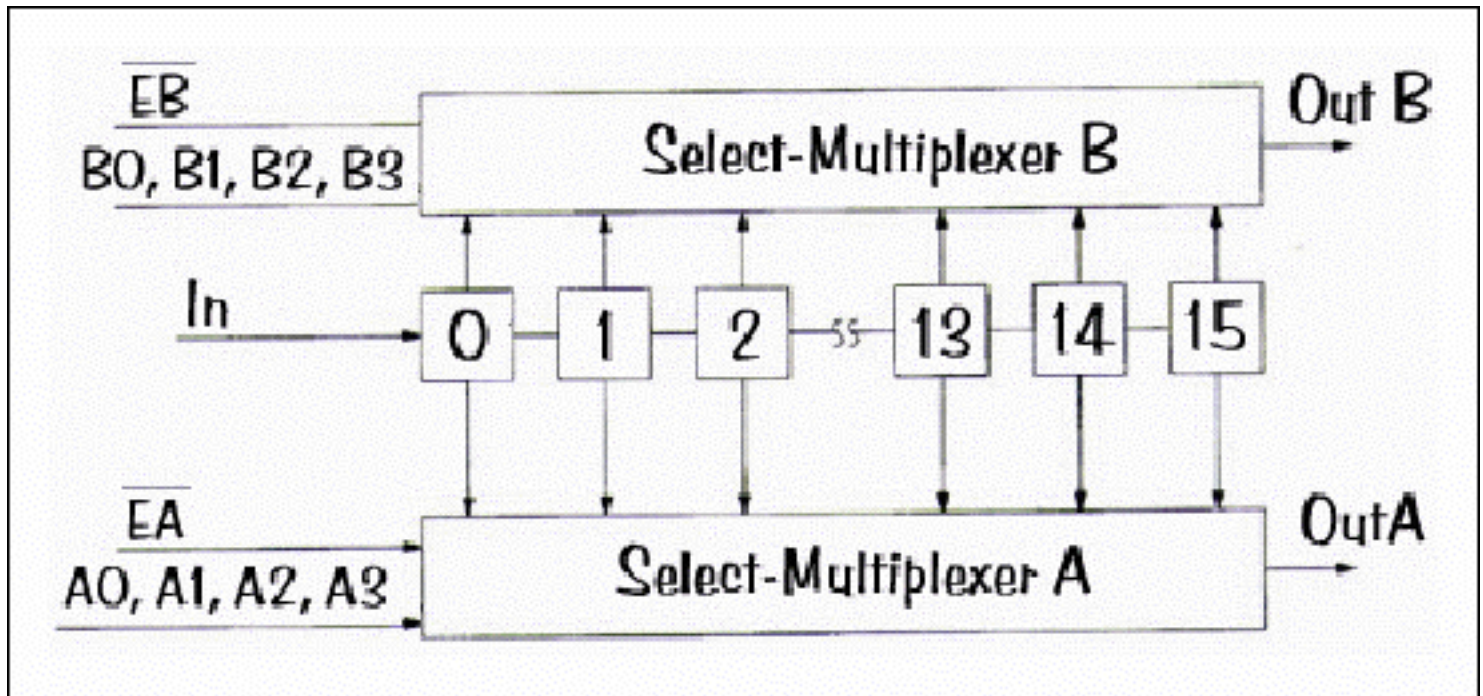


Figure 2.

Internally, it is equivalent to a 16-tap delay line with two multiplexers for selecting which taps are routed to the outputs. Each multiplexer has a 4-bit parallel input to select the required tap, so one byte of data could fully program the device.

In addition to the data sheet, there is additional characterization of this device in Application Note 421, [Device Characteristics of the DS1045 Dual 4-Bit Programmable Delay Line](#).

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