

APPLICATION NOTE 1775

Power Supply for DDR-SDRAM Termination Operates From 3V to 5.5V Input

Abstract: Double data rate (DDR) synchronous dynamic random access memory (SDRAM) has gained popularity recently. The DDR memory needs active termination, V_{TT}, that tracks the main memory voltage V_{DDQ}. This application note provides a switching regulator solution to provide a ½ tracking output for V_{TT} termination using MAX1957 pulse-width modulation (PWM) buck controller.

Double data rate (DDR) synchronous dynamic random access memory (SDRAM) has gained popularity because it can deliver double the data rate and reduced power consumption, compared to SDRAM at the same clock speed. These advantages come with more complex termination voltage requirements.

The DDR termination supply, V_{TT}, must now be capable of sourcing as well as sinking current. V_{TT} must track ½V_{DDQ}, the output supply voltage (currently V_{DDQ} is 2.5V, with ±3% accuracy). The input receiver is now a differential stage, requiring a reference bias, V_{TTR}, which must track the termination voltage V_{TT} to within ±40mV (refer to JEDEC standards JSD79 and JSD8-9).

Figure 1 is a typical output buffer and input receiver stage with series stub termination logic for 2.5V (SSTL-2) in a DDR_SDRAM single terminated system. For double termination, used in the case of a long bus, two R_T terminate each end of the bus.

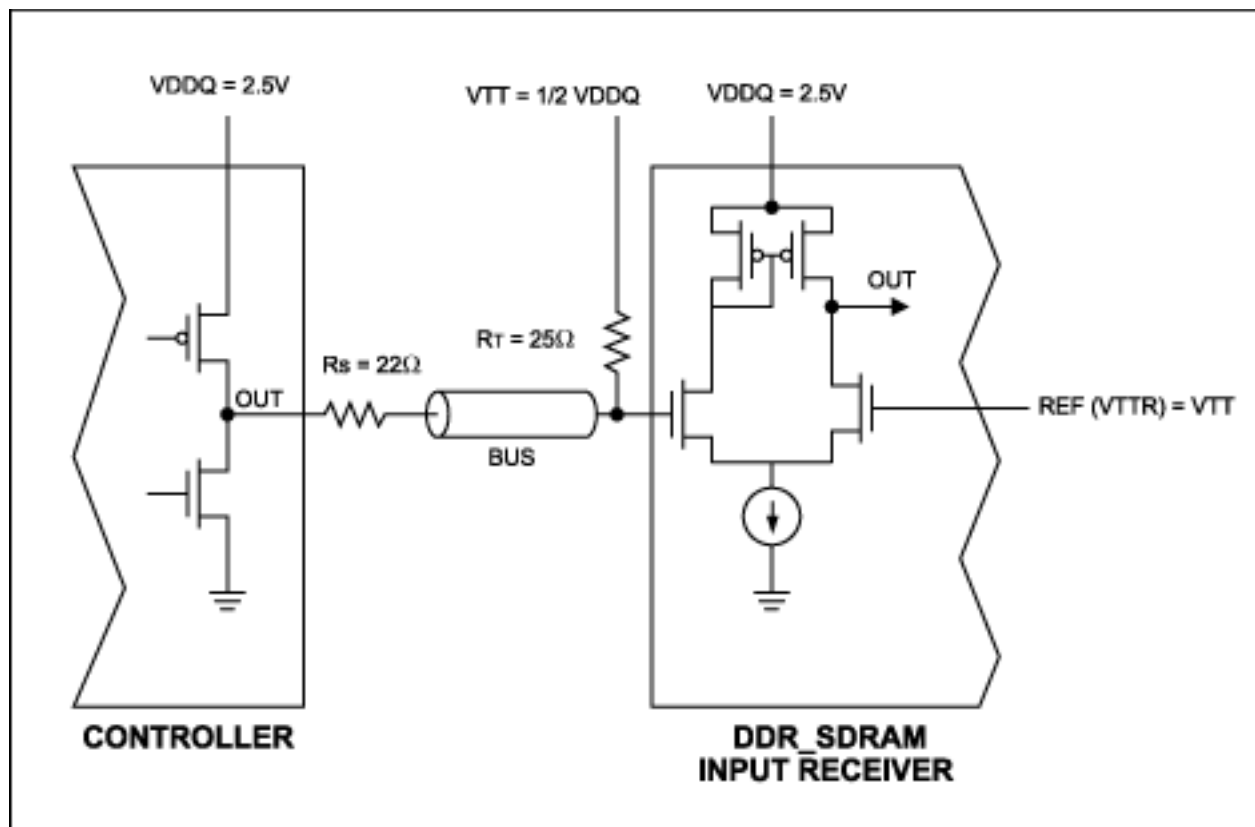


Figure 1. Single terminated SSTL-2 DDR_SDRAM system.

The MAX1957 circuit in **Figure 2** provides V_{TT} and V_{TTR} for DDR_SDRAM. The MAX1957 has a reference input (REFIN) that connects to the non-inverting input of the internal error amplifier to regulate the output V_{TT} to the same voltage as REFIN. To have V_{TT} and V_{TTR} track $\frac{1}{2}V_{DDQ}$, REFIN is developed by a resistor voltage divider (R1 and R2) from V_{DDQ} . Capacitor C6 is a decoupling filter. The MAX1957 operates as constant frequency PWM, such that V_{TT} can source and sink current as required by the DDR-SDRAM. Components used in Figure 2 provide over 3 Amperes of source and sink capability, which is the maximum requirement for a 128Mb memory system.

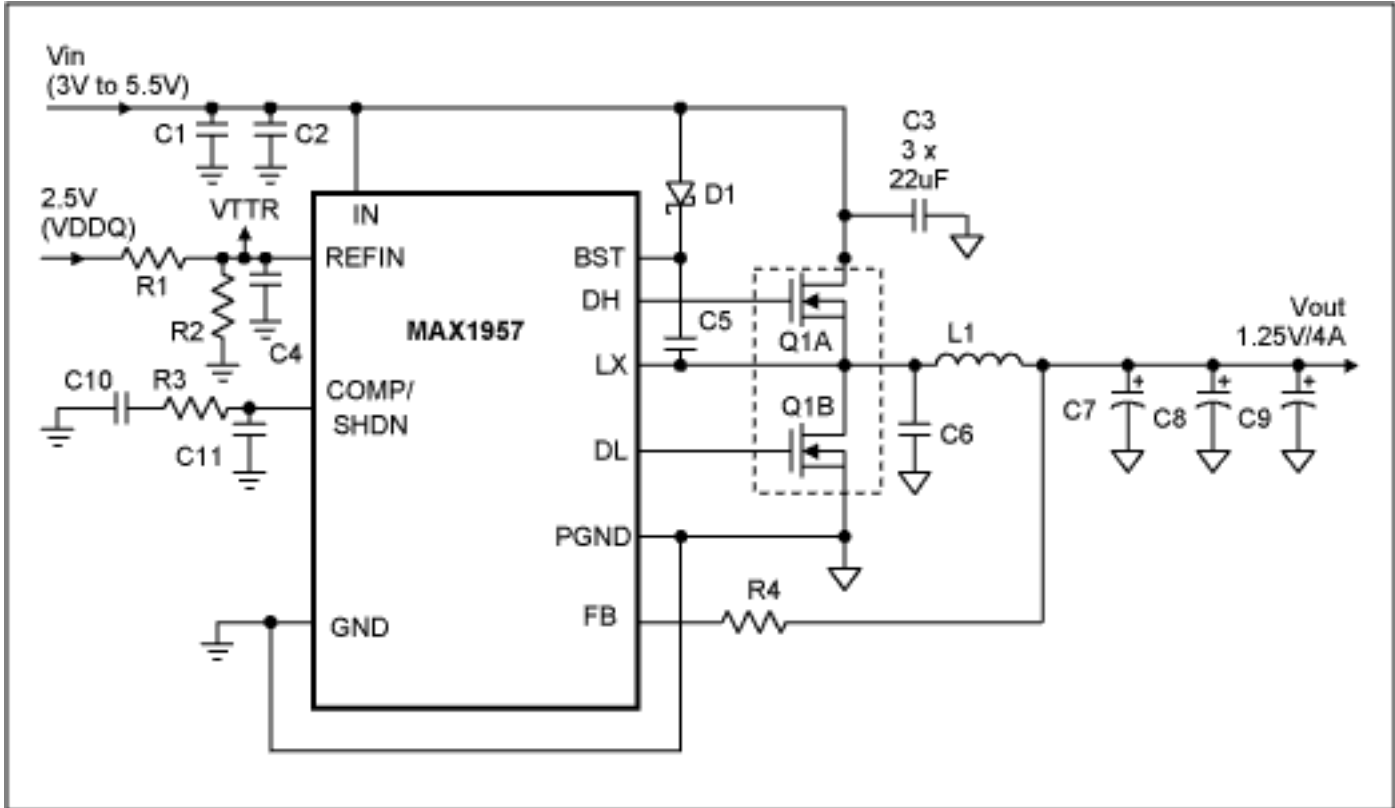


Figure 2. MAX1957 typical application circuit for V_{TT} and V_{TTR} .

Table 1. Component List for the MAX1957 Typical Application Circuit

Component	Quantity	Description
C1	1	Cap. 10 μ F/6.3V X5R Ceramic. Taiyo Yuden: JMK212BJ106MG
C2	1	Cap. 4.7 μ F/6.3V X5R Ceramic. Taiyo Yuden: JMK212BJ475MG
C3	3	Cap. 22 μ F/6.3V
C4,C5	2	Cap. 0.1 μ F/50V X7R Ceramic. Taiyo Yuden UMK107BJ104KA
C6	1	Cap. 1500pF/50V X7R Ceramic. Murata GRM89X7R152K50
C7, C8, C9	3	Cap. 270 μ F/2V SP Capacitor. Panasonic EEFUE0D271R
C10	1	Cap. 470pF/50V X7R Ceramic. Murata: GRM89X7R471K50
C11	1	Cap. 68pF/50V X7R Ceramic. Murata: GRM39COG680J50
D1	1	Diode, Schottky, 30V, 100mA, SOT-23. Central: CMPSH-3
IC	1	IC, Synch Buck controller: MAX1957
L1	1	Inductor, 2.7 μ H, 6.6A. Coilcraft: DO3316P-272HC
R1, R2	2	Resistor, 0805, 1K, 1%
R3	1	Resistor 51K, 0805, 5%
R4	1	Resistor 10K, 0805, 5%
Q1/2	1	Transistor, Dual MOSFET Fairchild FDS6890A 20V, 0.018 Ω

Figure 3 shows V_{TT} and V_{TTR} when subjected to a -3A to +3A step load at V_{TT} . The peak voltage deviation of V_{TT} is less than ± 40 mV.

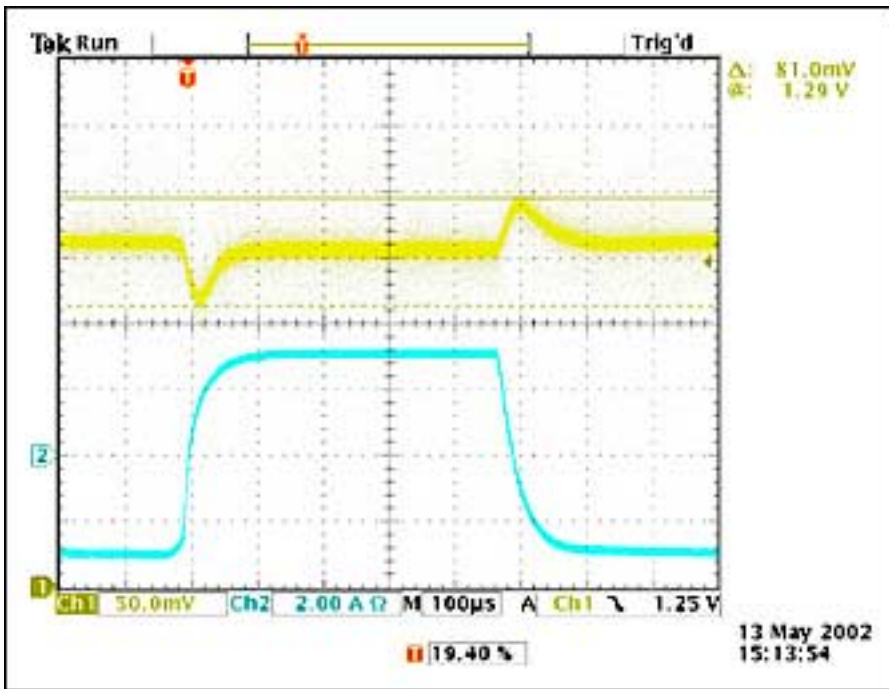


Figure 3. Top trace: voltage V_{TT} (AC coupled). Bottom trace: current I_{TT} step from -3A to +3A and from +3A to -3A.

Figure 4 shows V_{DDQ} , V_{TT} tracks to half of V_{DDQ} as V_{DDQ} ramps up and down, showing the change in V_{TT} is half of the change in V_{DDQ} .

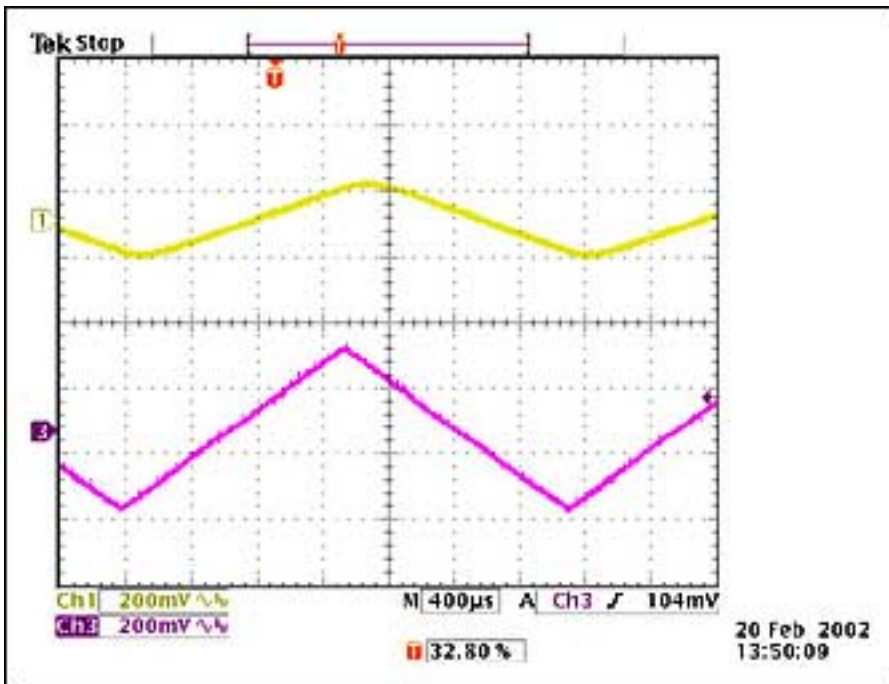


Figure 4. Top trace: voltage V_{TT} (AC coupled). Bottom trace: 2.5V V_{DDQ} (AC coupled).

It has been shown that the MAX1957 can be used as the controller for synchronous buck converter to provide termination voltage V_{TT} for DDR_SDRAM systems. For applications requiring higher current, the drive circuit of the MAX1957 is capable of driving large external power MOSFETs for output current up to 20A.

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