



APPLICATION NOTE 128

Testing and Calibrating a DS2760 Li-Ion Battery Monitor and Protector Based Circuit

Abstract: This application note describes to the reader how to properly test a circuit board and battery pack containing a Dallas Semiconductor DS2760 battery monitor and protector. A step-by-step test procedure is provided which can be followed to ensure that the circuit boards and battery packs have been assembled properly. Additionally, this note also instructs the reader on how to properly calibrate the high-accuracy current A/D converter on the DS2760 battery monitor once it is assembled into a battery pack. Procedures for both the current offset and current gain calibrations are covered.

Introduction

The advantages of lithium-ion protection and high accuracy fuel gauging can be completely negated by an assembly error or improper calibration of the device. This application notes walks through examples of how to test an assembled protection circuit board and a fully assembled pack followed by a step by step process to properly calibrate the DS2760's high accuracy Current A/D.

Performing a Board Level Test

The following is an example of how to production test a DS2760 based protection circuit board before final assembly into a cell pack. **Figure 1** shows a sample circuit board schematic utilizing all the DS2760's features. All critical test points (there are 11) are indicated with circled numbers in the figure. This test flow assumes all discrete components of the circuit have been tested and therefore the goal is to verify the board has been assembled properly by validating the connections.

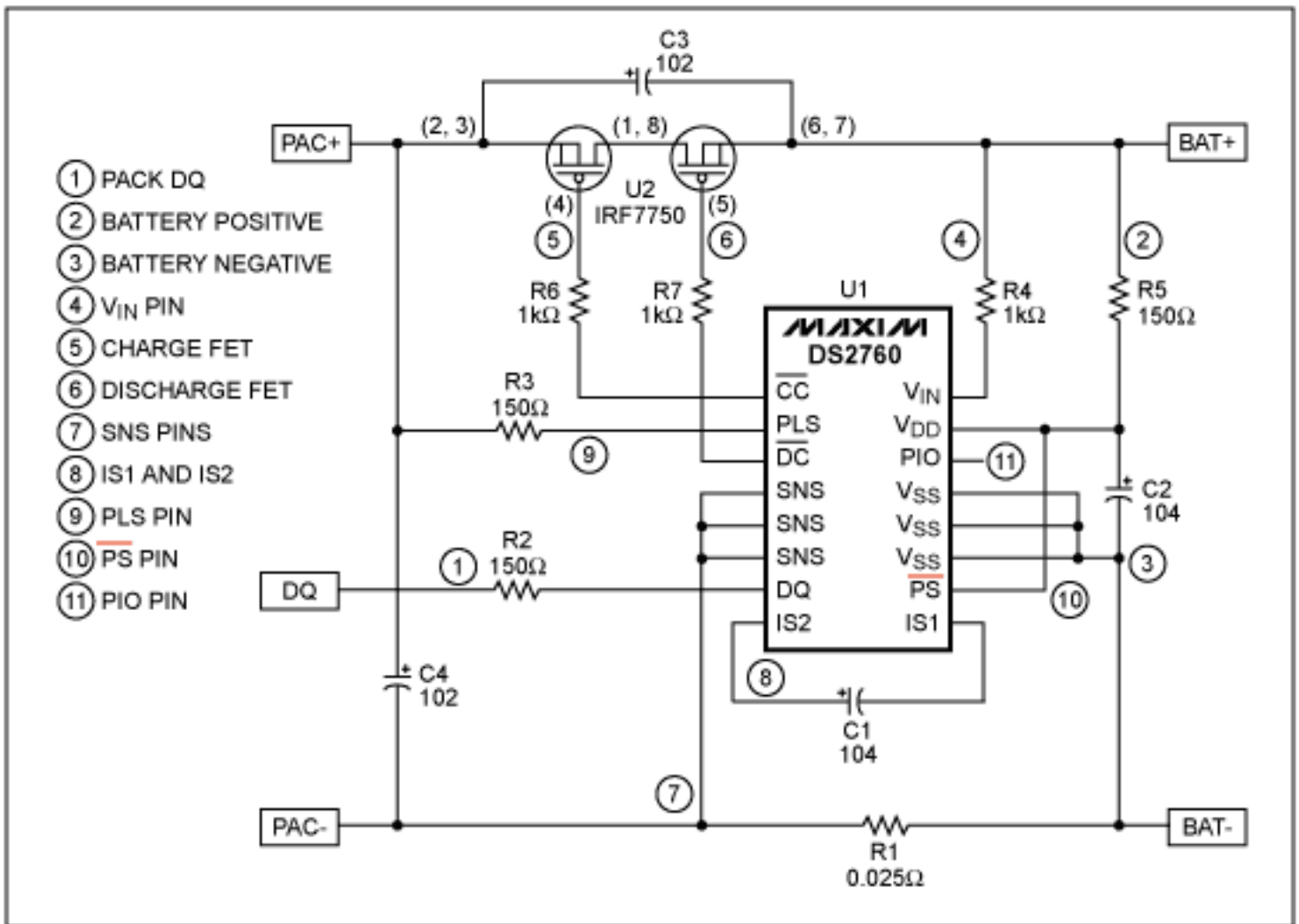


Figure 1. Circuit board nodes that must be verified.

Test 1: Test Initialization. The purpose of test initialization is to place the DS2760 registers into known states and determine there are any direct shorts on the board. Successful communication to the device in this step verifies the DQ connection (node 1) as well as Battery Positive to the VDD pin (node 2) and Battery Negative to the VSS pin and PAC- (node 3). The charge and discharge FETs are enabled then the Protection Register is checked for flag conditions:

- Force 4.0V from BAT+ to BAT-
- Write 0x00h to the Protection Register Clear all flags
- Write 0x03h to the Protection Register Enable FETs
- Wait 150 ms Wait for test of all possible flag conditions
- Read the Protection Register Read DOC flag

Fail board if DOC Flag (bit 4) is set.
 Fail board if communication is not possible.

Test 2: Verify VIN pin connection to Battery Positive (node 4). Read the latest voltage from the DS2760 and confirm it is a valid measurement:

- Force 4.0V from BAT+ to BAT-
- Wait 10 ms Wait for voltage conversion
- Read Voltage Register 2 Bytes

pack is shown in **Figure 2**. All critical test nodes are indicated with a circled number.

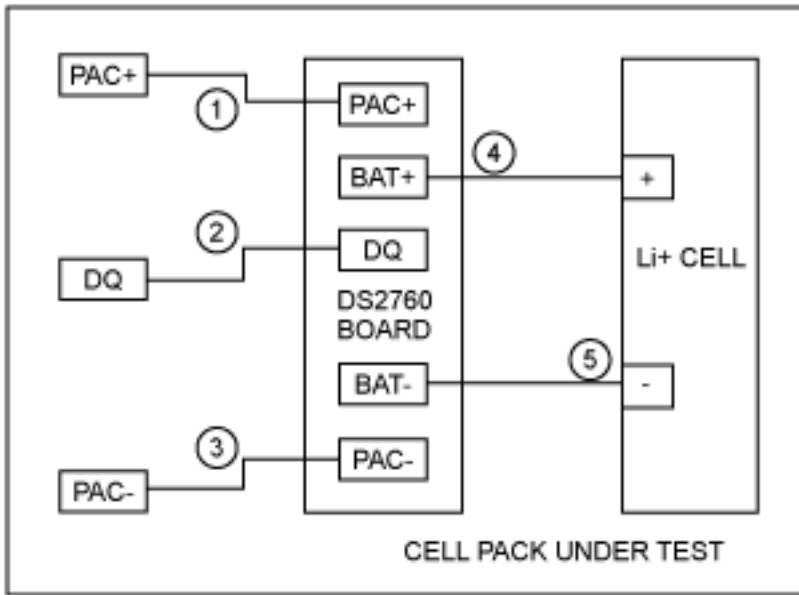


Figure 2. Cell pack nodes that must be verified.

Test 1: Communication. The simple act of reading the DS2760's net address verifies most of the connections in this circuit. For proper communication, the DQ pin (node 2) and PAC- (node 3) must be valid connections. For the DS2760 to properly respond, the board must be powered through BAT+ (node 4) and BAT- (node 5). The communication test is:

Read the Net Address

Fail pack if communication is not possible.

Test 2: Power. To verify that PAC+ is properly connected to the DS2760 board, enable the FETs and verify that the cell voltage can be measured on the PAC+ pin. Also check the DS2760 to see if any short circuits were detected:

Write 0x00h to the Protection Register Clear all flags

Write 0x03h to the Protection Register Enable FETs

Wait 150ms

Wait for test of all possible flag conditions

Read the Protection Register

Read DOC flag

Fail pack if DOC Flag (bit 4) is set.

Fail pack if cell voltage cannot be measured at PAC+

Test 3: PIO and PS. If pack design uses the PIO and PS pins as inputs or outputs, verify their operation by toggling pin states and confirming the results in the Special Feature Register. See test steps 7 and 8 in the board level test section above.

Calibrating the Current Offset

The current A/D of the DS2760 is extremely sensitive. It is capable of measuring a voltage drop of only 15 μ V across the sense resistor. This kind of accuracy can only be achieved by calibrating the current measurement after the cell pack is assembled. The current offset register allows the current measurements of the DS2760 to be adjusted by ± 127 LSbs for accurate measurement of very small currents. The following example lists the steps to calibrate the DS2760 in circuit:

1. Write 0x00 to the Protection Register to disable all charging and discharging.
2. Average 32 current measurements with at least a 100 ms interval between samples. It is recommended

- to use many readings as possible for best accuracy.
3. If the averaged current register value is greater than ± 127 LSbs ($\pm 79.375\text{mA}$ or $\pm 1.984\text{mV}$) the device cannot be trimmed to zero. Verify circuit.
 4. Store the resulting value in the Current Offset Register location 0x33h and copy to EEPROM.
 5. Verify accuracy with additional current measurements. Repeat process if necessary.

Calibrating the Current Gain

DS2760s with integrated sense resistors are calibrated at the factory to accurately report current, no further calibration is necessary. The DS2760 without integrated sense resistor will be factory calibrated to measure voltage. To accurately convert this voltage value into a current reading, the exact sense resistance must be known. Dallas Semiconductor recommends measuring this resistance at pack assembly and storing the value in EEPROM for reference by the handset. A sample procedure for this process would be as follows:

1. Accurately measure the sense resistance of the assembled circuit. This can be accomplished by forcing a known current through the pack and using the DS2760 to measure the voltage drop across the sense resistor.
2. Store the resistance value in unused DS2760 EEPROM. Dallas Semiconductor recommends storing with at least 0.25m Ω resolution. One byte would provide a range of 0m Ω to 63.75m Ω .
3. During operation, the handset reads this resistance value and multiplies the Current Register and Current Accumulator values with it to calculate the measured current and accumulated charge.

Summary

Proper verification of an assembled DS2760 based lithium-ion cell pack requires testing of every solder point in the circuit. At the very minimum, the test should verify that the protection prevents all current flow into and out of the pack when the control FETs are disabled.

The Current A/D offset should be calibrated after assembly into the pack. For greatest accuracy, multiple measurements should be made over the longest acceptable period of time while the control FETs are disabled guaranteeing no current flow in the system.

Application Note 128: <http://www.maxim-ic.com/an128>

More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

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Related Parts

DS2751: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

DS2760: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS2761: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

DS2762: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

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