Keywords: DDR Memory-Termination Supply

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APPLICATION NOTE 1149

DDR Memory-Termination Supply

The high-speed memory of workstations and servers contains double data rate (DDR) synchronous DRAMs (SDRAMs). These memory ICs operate with supply voltages of 2.5V or 1.8V, and require a reference voltage equal to half the supply voltage (V_{REF} = 1/2V_{DD}). Their logic outputs connect via resistors to a termination voltage V_{TT}, which is equal to and tracks VREF. That is, V_{TT} must source or sink current as required while maintaining V_{TT} = V_{REF} ±0.04V.

The circuit of **Figure 1** provides this V_{TT} termination voltage (with 6A source/sink capability) for both 2.5V and 1.8V memory systems. U1 is a low-voltage stepdown controller whose minimum operating voltage (3.15V) is compatible with the 3.3V I/O-logic supply found in most computer systems. U1's forced-PWM mode of operation can sink or source output current as required to maintain the regulated output voltage, and its maximum sink current equals its maximum source current. (When sinking current, it returns some current to the input supply).

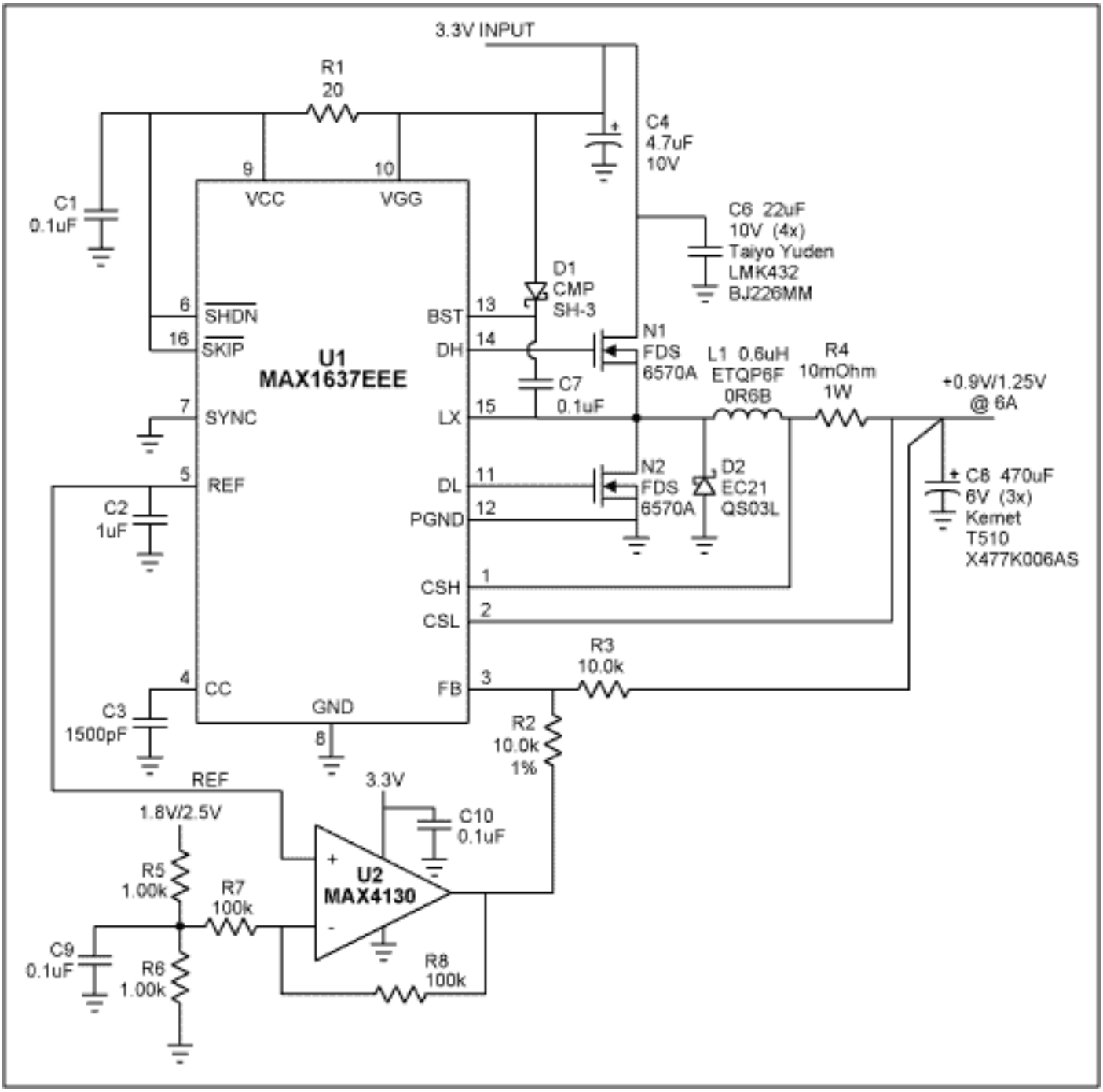

Figure 1. This DDR memory-termination supply can source and sink 6A while maintaining a regulated $1/2V_{DD}$ (for 1.8V or 2.5V supplies).

Op amp U2 compares $1/2V_{DD}$ (created by R5 and R6) with V_{REF} from U1, and produces an error signal that is applied through R2 to U1's feedback terminal (pin 3). That action forces the V_{TT} output (0.9V in this case) to track $1/2V_{DD}$. U2 has the performance necessary for this application: low input-offset voltage, low input bias current, and rail-to-rail-output capability. To deliver $1/2V_{DD}$ to the memory system, you may need to add a buffer to the R5/R6 divider.

Application Note 1149: http://www.maxim-ic.com/an1149

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AN1149, AN 1149, APP1149, Appnote1149, Appnote 1149